EE 393 LAB 5

1. Design a Schmitt Trigger input buffer with V_{th} = 2.5 V for rising input (0 to 5 V) and V_{th} = 1.4 V for falling input (5 to 0 V). Work with the given PSpice schematic file using the T15D Process from MOSIS. The buffer should be able to source and sink 4 mA.

2. Create a ***block diagram*** (perhaps using Visio) showing how you would combine the circuit from step 1 with appropriate modifications to the BiCMOS circuit from lab 4 to create a 1-bit transceiver. The transceiver is a part of a bidirectional data bus. Two signals, ~CS (Chip select) and R/~W (Read/Write not), must be used to control the flow of data through the bidirectional data bus (details in table below). ***Include*** the logic (at the logic gate level) for generating the Z (output buffer tristate control) signal from the ~CS and R/~W bus signals.

~CS	**R/~W**	**Output Mode**
1	X	High Z
0	1	Normal Operation, Data can be put into the bus
0	0	High Z, Data will be written into memory by the CPU

Report Requirements

- Part 1
  - Show that V_{th} meets the spec through **DC analysis** (Excel method, or "slow" transient analysis with V_{in} on x-axis in PSpice – watch your response time).
  - Correlate the results of DC analysis with a transient analysis of the circuit using a 10 MHz pulse ($T_r = T_f$ = 15 ns) using a 20 pF load. Adjust the frequency, load, and rise/fall times as needed to demonstrate the 2 values of V_{th}.
- Part 2
  - Objective – Define the problem. Provide a top-level system diagram.
  - Submit the truth table and combinational (gate) logic circuit for generating the Z control signal.

Due Week 10