EE 393 **LAB 4**

1. Design a single inverter CMOS output stage, such that t_d (delay time) is 20 ns $\pm$ 10% for C_L = 50 pF. Delay time is defined as the time between the input reaching $V_{DD}/2$ and the output reaching $V_{DD}/2$. For this step, the input is voltage into the output stage and the output is the load capacitor.

2. To your circuit from step 1, add your previously designed IBUF (V_{inv} = 1.4 V $\pm$ 10%) and your previously designed core logic inverter. Find the overall delay time for this circuit.

3. Now, between the core and the final output stage, add 1 or more inverting stages as needed in a super buffer configuration. Find the overall delay time for this circuit and compare to part 2. (It should go down.)

4. Design a BiCMOS inverter for driving a capacitive load of 50 pF. The maximum frequency of operation must exceed 25 MHz. Simulate using PSPICE.

5. Tristate the output of part 4 by effectively grounding the base current of the BJTs per a tristate control signal. The NMOS transistor that grounds the base of the sourcing BJT must be sized large enough so that it pulls the base below 0.7 V (it forms a voltage divider with the PMOS of the inverter when the inverter output is a logic 1).

Note: For each circuit, you may need to add an extra core inverter to ensure the overall circuit is an inverter.

Use the T15D model from MOSIS (λ= 0.30 μm) for the NMOS and PMOS transistors.

Use the following model, available at http://iesg.eecs.berkeley.edu/ee105/Overview.fm5.html and on the course website, for the bipolar transistor:

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*Bipolar Transistors

*3505S (similar to 3500, 3501) vertical NPN

.model 3505S NPN IS=5.65E-17 RB=465 RE=0.495 RC=41.5 CJE=0.555p
+CJC=0.155p CJS=0.205p BF=94.5 VAF=50.0 BR=0.720 VAR=4.40 VJE=0.960
+MJE=0.330 VJC=0.730 MJC=0.520 VJS=0.450 MJS=0.330 TF=39.0p TR=1.00n
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PSPICE Note: PSPICE does not like model names starting with a numeric character. The first character in a model name must be an alphabetic character. Add the letter B for Bipolar in front of the model name.

Report Requirements:

1. Show design calculations.
2. Submit all schematics.
3. Submit DC transfer curves for both the overall super buffer circuit and the BiCMOS circuit.
4. Display the I_{DS} and V_{DS} curves vs. time for both PMOS and NMOS output transistors and label the max current. Display a similar graph for the BiCMOS circuit.
5. Based on the calculated delay time for the 2 main circuits, determine the maximum frequency of operation for the specified load.
6. Discuss results

Due: Friday of Week 8 (for both sections)