EE 393 **LAB 3**

1. Design a CMOS transmission gate using minimum geometry transistors. Select L = 2λ, W_n = 4λ and adjust W_p such that both PMOS and NMOS transistors have the same β_p and β_n.

   W_n and W_p are the widths of NMOS and PMOS transistors, respectively.

2. Using the transmission gate described in part 1, design a 2:1 Multiplexer core logic section.

3. Design a 2:1 multiplexer chip by adding I/O.
   1. Add in input buffers to each input signal so that V_{inv} = 1.4V ± 10%
   2. Add an output buffer to so as to provide 2 mA ± 10%
4. Do the layout of the 2:1 Multiplexer chip using Microwind
5. Verify the performance of the circuit with and without the parasitics taken from your physical layout

   Use T15D process from MOSIS (λ = 0.30 μm)

   Measure current delivered by circuit 1

   Find the maximum frequency of operation of the core logic circuit for 1 pF capacitive load.

   Because of the 10-transistor limitation of the student version of the PSPICE package, simulate only the core logic together with the output stage. (You will design the input stages in Microwind, but not simulate them.)

Report Requirement:

1. Submit schematics and graphs that show the performance of the circuit.
2. Submit the layout of the chip
3. Discuss results.

Due Week 7