EE 393 **LAB 1**

1. Develop the I_{ds}, V_{ds} family of curves for a NMOS. Use W = 4λ and the length of each active region = 5λ
2. Develop the I_{ds}, V_{ds} family of curves for a PMOS. Use W = 4λ and the length of each active region =5λ
3. Increase the width of the PMOS transistor so that the I_{ds}, V_{ds} family of curves matches with that of 1 for Vgs = 5 v, Vds = 5 V within ± 10 %. Use PSPICE only
4. Combine the NMOS transistor of 1 and PMOS transistor of 3 to obtain a CMOS inverter.
5. For the CMOS inverter of 4 determine the transition voltage (Vth) and the rise and fall time for a 2 pf load using 5V pulses of frequency 1 MHz and 10 MHz.

Use T15D process from MOSIS and use λ = 0.3 μm for all parts.
For all parts do simulation with PSPICE using Level 3 Model

Report Requirement:

1. Submit Transistor characteristic (Id vs. Vds) curves. Label them with Vgs and indicate maximum current from PSPICE only (parts 1, 2 and 3).
2. For part 4 submit Inverter transfer characteristic and show the transition voltage and label the transition voltage from PSPICE only.
3. For part 5 submit input voltage and output voltage and current waveforms for nominal case (1 MHz) and the limiting case (10 MHz) from PSPICE only.
4. Submit all the schematics for parts 1 through 5. Indicate the Length and Width values on the schematics.

Parameter	Level 3 Model Use PSPICE
gds of Pmos @Vds =VGS = - 5V	
Ids of Nmos @Vds =VGS = 5V	
Isd of Pmos @Vds =VGS = -5V	
Vth for part 4	

1. For part 3, show the width computation for equal current and for part 4 compute the expected transition voltage (Vth) and compare it with the actual transition voltage (Vth)
2. Add a cover sheet with your name.

Due Date: Week 3