Timers on the 68HC11

- Always-running counter (2 MHz, 16-bit)
- Port A (0x1000): I (0-2), O (3-6), I/O (7)
- Main functions
  - Output compare: set flag (optional interrupt) when timer reaches a certain value
    - Can also automatically set/clear/toggle output bits
  - Input capture: set flag (optional interrupt) when input bit rises/falls
    - Also record timer value
  - Pulse accumulator: count external events
  - Real-time interrupt: periodic interrupt generator

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Example of Real-time interrupt

- Interrupt vector jump table for Real-Time Interrupt (RTI) is at 0xEB-0xED
- Interrupt rate is set in pactl (0x1026)
- Must also set RTI bit in tmsk2 (0x1024)
- Must clear RTI flag in tflg2 (0x1025) after each RTI
  - Flag is cleared by writing a 1 to that bit

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tmsk2

	7	6	5	4	3	2	1	0	
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
RESET	0	0	0	0	0	0	0	0	

TOI — Timer Overflow Interrupt Enable
0 = TOF interrupts disabled
1 = Interrupt requested when TOF = 1

RTII — RTI Interrupt Enable
0 = RTIF interrupts disabled
1 = Interrupt requested when RTIF = 1

PAOVI — Pulse Accumulator Overflow Interrupt Enable
0 = PAOVF interrupts disabled
1 = Interrupt requested when PAOVF = 1

PAII — Pulse Accumulator Input Interrupt Enable
0 = PAIF interrupts disabled
1 = Interrupt requested when PAIF = 1

Bits 3 and 2 — Not Implemented
These bits always read zero.

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tmsk2 – continued

PR1 and PR0 — Timer Prescaler Selects

These two bits may be read at any time but may only be written during initialization. Writes are disabled after the first write or after 64 E cycles out of reset. If the MCU is in special test or special bootstrap mode, then these two bits may be written any time.

These two bits specify the timer prescaler divide factor.

PR1	PR0	Prescaler
0	0	÷ 1
0	1	÷ 4
1	0	÷ 8
1	1	÷ 16

Use 'I' command in WBUG11 to set this for Fox11 (in normal expanded mode)

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tflg2

	7	6	5	4	3	2	1	0	
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2
RESET	0	0	0	0	0	0	0	0	

TOF — Timer Overflow

This bit is cleared by reset. It is set to one each time the 16-bit free-running counter advances from a value of $FFFF to $0000. This bit is cleared by a write to the TFLG2 register with bit 7 set.

RTIF — Real Time Interrupt Flag

This bit is set at each rising edge of the selected tap point. This bit is cleared by a write to the TFLG2 register with bit 6 set.

PAOVF — Pulse Accumulator Overflow Interrupt Flag

This bit is set when the count in the pulse accumulator rolls over from $FF to $00. This bit is cleared by a write to the TFLG2 register with bit 5 set.

PAIF — Pulse Accumulator Input Edge Interrupt Flag

This bit is set when an active edge is detected on the PAI input pin. This bit is cleared by a write to the TFLG2 register with bit 4 set.

Bits 3-0 — Not Implemented

These bits always read zero.

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pactl

	7	6	5	4	3	2	1	0	
$1026	DDRA7	PAEN	PAMOD	PEDGE	0	0	RTR1	RTR0	PACTL
RESET	0	0	0	0	0	0	0	0	

DDRA7 — Data Direction for Port A Bit 7

0 = Input only

1 = Output

PAEN — Pulse Accumulator System Enable

0 = Pulse accumulator off

1 = Pulse accumulator on

PAMOD — Pulse Accumulator Mode

0 = External event counting

1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control

This bit has different meanings depending on the state of the PAMOD bit.

PAMOD	PEDGE	Action on Clock
0	0	PAI Falling Edge Increments the Counter
0	1	PAI Rising Edge Increments the Counter
1	0	A zero on PAI Inhibits Counting
1	1	A one on PAI Inhibits Counting

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pactl – continued

Bits 3-2 — Not Implemented
These bits always read zero.

RTR1 and RTR0 — RTI Interrupt Rate Selects
These two bits select one of four rates for the real time periodic interrupt circuit (see **Table 8-1**). Reset clears these two bits and after reset, a full RTI period elapses before the first RTI interrupt.

Table 8-1 Real Time Interrupt Rate versus RTR1 and RTR0

RTR1	RTR0	Rate	XTAL = 12.0 MHz	XTAL = 2^{23}	XTAL = 8.0 MHz	XTAL = 4.9152 MHz	XTAL = 4.0 MHz	XTAL = 3.6864 MHz
0	0	$2^{13} \div E$	8.192 ms	3.91 ms	4.10 ms	6.67 ms	8.19 ms	8.89 ms
0	1	$2^{14} \div E$	16.384 ms	7.81 ms	8.19 ms	13.33 ms	16.38 ms	17.78 ms
1	0	$2^{15} \div E$	32.768 ms	15.62 ms	16.38 ms	26.67 ms	32.77 ms	35.56 ms
1	1	$2^{16} \div E$	65.536 ms	31.25 ms	32.77 ms	53.33 ms	65.54 ms	71.11 ms
		E =	3.0 MHz	2.1 MHz	2.0 MHz	1.2288 MHz	1.0 MHz	921.6 kHz

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RTI example description

- Start at 01, count up to BCD overflow
- Increase count once per second
- Display will stop at 99

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Program outline

- Main program sets up then
  - display number until number == 0
  - number is read by main, written by interrupt service routine
- Interrupt service routine (ISR) gains control when real time interrupt (RTI) fires
  - Will count 61 times through for 1 second

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RTI example

- Example code on website
  - rti.s

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Example details

- Why the 61?
  - 16.38 ms x 61 counts = 0.99918 seconds
  - Only a 0.82 ms error
  - Close enough for our purposes
- More accurate than timing loops

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References for Final Lab

- Output compare system
  - Motorola Reference Manual (Rev. 6)
    - Sections of Chapter 10
      - 10.2, 10.3 (skim figure 10-1)
      - 10.4
        - focus on logic/registers
        - skip or skim timing/circuits, skip 10.4.3
        - Table 10-1 (briefcase crystal is 8 MHz)
      - 10.6 (skip 10.6.2 and 10.6.3)

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