CS-280: Successive Approximation for Analog to Digital (A/D) Conversion

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Introduction

The analog to digital (A/D) conversion system of the M68HC11 uses a network of switchable capacitors to successively approximate an analog input voltage. The capacitors are arranged in powers of 2, starting with two 1-unit capacitors (1, 1, 2, 4, 8, ..., 2^{N-1}). Note that the sum of the capacitances is 2^N times some constant value given in Farads, where N is the number of bits of resolution. The exact capacitances are not important for understanding the basic, static operation of the circuit.

Briefly, the A/D conversion proceeds as follows. First, an analog input voltage is used to charge several capacitors in parallel. The total capacitance (found by adding the individual capacitances) and input voltage determine the total charge, which is constant throughout the conversion. Second, the input voltage is disconnected and the circuit is reconfigured so that the negative input to a comparator is the negative of the analog input voltage. Third, starting with the largest capacitor (MSB), one terminal of each capacitor is moved from ground to logic 1 (normally 5 V) and the output of the comparator is examined to determine whether the corresponding output bit should be a 1.

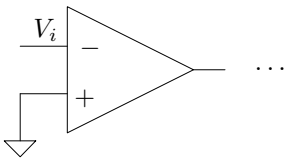
This is analogous to making change. We start with the largest denomination (MSB) and keep adding one unit (voltage resulting from charge on a capacitor) as long as the accumulated total (input to the comparator) does not exceed the total we are seeking (original analog input voltage). Since the units of "currency" are arranged in powers of 2 in the A/D converter, it turns out that we will need exactly 0 or 1 of each unit.

For example, if we have a 4-bit A/D converter and our largest analog input is 5 V, the units are 2.5 V, 1.25 V, 0.625 V, and 0.3125 V.

Additional circuitry (for protecting the circuit from high input voltages, switching the capacitors, etc.) is needed to make a complete successive approximation A/D converter.

Background – Comparator

A comparator takes two analog input voltages and outputs logic 1 if the positive input is greater than the negative input. Otherwise, the output is logic 0.

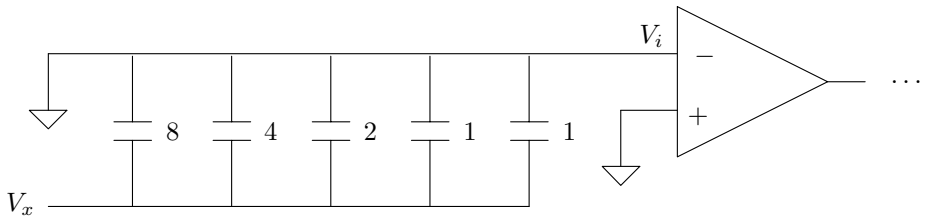


Comparator output: logic 0 if $V_i > 0$
logic 1 if $V_i < 0$

Step 1 – Charge Capacitors Using Voltage To Be Converted

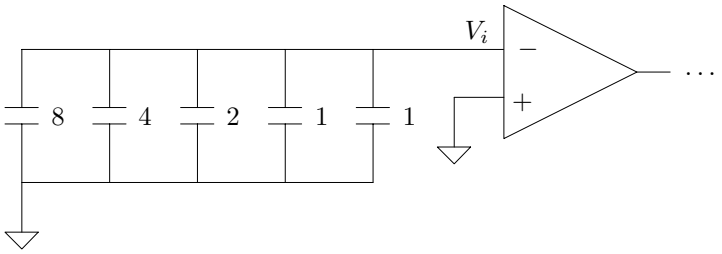
The following example is based on Section 12 of the Motorola 68HC11 Reference Manual.

$$V_H = 5.0 \text{ V (logic high)}$$
$$\text{Example: } V_x = \frac{21}{32}V_H = 3.28125 \text{ V (analog voltage to convert)}$$



Charge: $Q_s = (8 + 4 + 2 + 1 + 1)(V_x - 0) = 16V_x = \frac{21}{2}V_H$

Step 2 – Disconnect Top Plates From Ground, Disconnect V_x, and Connect Bottom Plates to Ground



Charge is conserved, so $V_i = -V_x$.

Step 3 – Approximate V_i Beginning With MSB

Starting with MSB ($C = 8$) flip *lower* plate from 0 V to $V_H = 5\ V$.

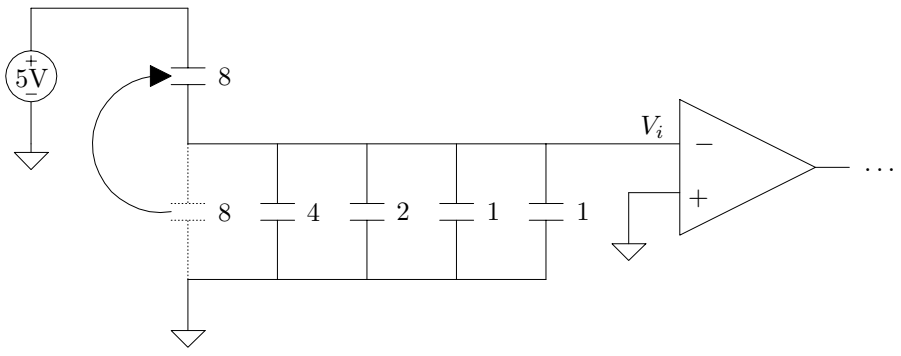
If $V_i < 0$ (comparator output is 1), proceed to next bit. Otherwise, flip capacitor back to original position and go to next bit.

$$\begin{aligned} C_{top} &= \sum \text{Parallel capacitances on top } (V_i \text{ to } 5 \text{ V}) \\ C_{bot} &= \sum \text{Parallel capacitances on bottom } (V_i \text{ to } 0 \text{ V}) \end{aligned}$$

$$\begin{aligned} \text{Charge: } Q &= C_{top}(V_H - V_i) + C_{bot}(0 - V_i) \\ &= C_{top}V_H - (C_{top} + C_{bot})V_i \end{aligned}$$

Note: $C_{top} + C_{bot} = 16 = 2^4 = 2^N$, where N is the number of bits.

Flip first capacitor ($C = 8$)...



$$
\begin{aligned}
Q &= C_{top}V_H - (C_{top} + C_{bot})V_i \\
&= 8V_H - 16V_i \\
\text{Charge conserved: } Q_s &= Q \\
\frac{21}{2}V_H &= 8V_H - 16V_i \\
\frac{5}{2}V_H &= -16V_i \\
-\frac{5}{32}V_H &= V_i
\end{aligned}
$$

$V_i < 0 \therefore$ comparator output (MSB of result) is 1 $\therefore$ leave capacitor up

When we move 2nd capacitor up:

$$
\begin{aligned}
Q &= C_{top}V_H - (C_{top} + C_{bot})V_i \\
&= (8+4)V_H - 16V_i \\
\frac{21}{2}V_H &= 12V_H - 16V_i \\
-\frac{3}{2}V_H &= -16V_i \\
\frac{3}{32}V_H &= V_i
\end{aligned}
$$

$V_i > 0 \therefore$ comparator output (2nd MSB of result) is 0 $\therefore$ put capacitor down

So far, we have 10_2. The next two bits are 1 and 0, so we end up with $1010_2 \ldots$

$$
\begin{aligned}
C_{top} &= 8 + 2 = 10 \\
Q &= 10V_H - 16V_i \\
\frac{21}{2}V_H &= 10V_H - 16V_i \\
\frac{1}{2}V_H &= -16V_i \\
-\frac{1}{32}V_H &= V_i
\end{aligned}
$$

This final value of V_i is the error of the approximation. Even assuming no noise, we have converted a continuous value to a value having 16 levels, so some precision was lost. The error computed this way will be between 0 and -1 LSB.

To get a better approximation, we add $\frac{V_H}{2^{N+1}} = \frac{5}{32}$ V to our estimate for V_x. Since 0000_2 corresponds to the range from 0 to $\frac{V_H}{2^N} = \frac{5}{16}$ V, the best estimate for the corresponding voltage is in the middle of the range.

So, our final estimate is $V_x' = (\frac{1010_2}{10000_2} + \frac{1}{32})V_H = \frac{21}{32}V_H$, which happens to be exactly equal to V_x in this case.