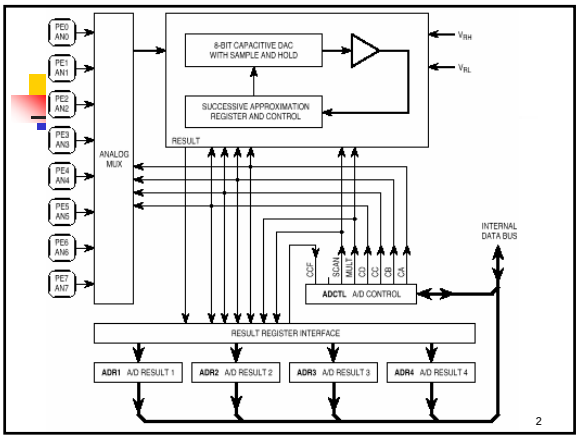
Port E - 0x100A

- A/D (analog to digital) and digital in
- Motorola – “Digital reads of port E pins are not recommended during the sample portion of an A/D conversion cycle.”

1



2

OPTION, A/D power up

$1039	ADPU	CSEL	IRQE	DLY	CME		CR1	CR0	OPTION	System Configuration Options

- OPTION, 0x1039
- Bit 7, ADPU, the A/D power up bit
- 1 = A/D powered up
- Only change that bit

3

A/D power up code

```
OPTION = 0x1039
…
ldaa OPTION
oraa #0b10000000 ;set bit 7
staa OPTION      ;change it
…
```

4

ADCTL

- CCF – conversion complete flag
- SCAN
  - 0 = 4 conversions and stop
  - 1 = continuous
- MULT
  - 0 = single channel
  - 1 = four channels in range

Address: $1030

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CCF	0	SCAN	MULT	CD	CC	CB	CA
Write:								
Reset:	0	0	U	U	U	U	U	U

U = Unaffected

Figure 12-6. A/D Control/Status Register (ADCTL)

Reference Manual M68HC11 — Rev. 5

5

Table 12-1. A/D Channel Assignments

CD	CC	CB	CA	Channel Signal	Result in ADRx if MULT = 1
0	0	0	0	PE0	ADR1
0	0	0	1	PE1	ADR2
0	0	1	0	PE2	ADR3
0	0	1	1	PE3	ADR4
0	1	0	0	PE4*	ADR1
0	1	0	1	PE5*	ADR2
0	1	1	0	PE6*	ADR3
0	1	1	1	PE7*	ADR4
1	0	0	0	Reserved	ADR1
1	0	0	1	Reserved	ADR2
1	0	1	0	Reserved	ADR3
1	0	1	1	Reserved	ADR4
1	1	0	0	V_H**	ADR1
1	1	0	1	V_L**	ADR2
1	1	1	0	1/2 V_H**	ADR3
1	1	1	1	Reserved**	ADR4

*Not available in 48-pin package versions
**These channels intended for factory testing

M68HC11 — Rev. 5 Reference Manual

6

A/D results

$1030	CCF		SCAN	MULT	CD	CC	CB	CA	ADCTL	A/D Control Register
$1031	Bit 7	–	–	–	–	–	–	Bit 0	ADR1	A/D Result Register 1
$1032	Bit 7	–	–	–	–	–	–	Bit 0	ADR2	A/D Result Register 2
$1033	Bit 7	–	–	–	–	–	–	Bit 0	ADR3	A/D Result Register 3
$1034	Bit 7	–	–	–	–	–	–	Bit 0	ADR4	A/D Result Register 4

7

A/D voltage

- Q is a quantum (voltage step)
- Q = (Vmax – Vmin) / 2^n
- Q = (5 – 0)/2^8 = 5/256 = 19.53125 mV
- Voltage read = Q * number
- If number = 0x10000000 what is the voltage?
  - V = Q * 128 = 2.5 V

8

A/D implementation

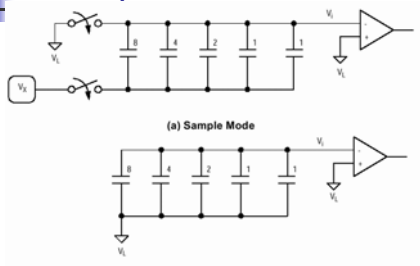


Figure 12-1. Basic Charge-Redistribution A/D

M68HC11 — Rev. 5 Reference Manual

9

A/D timing

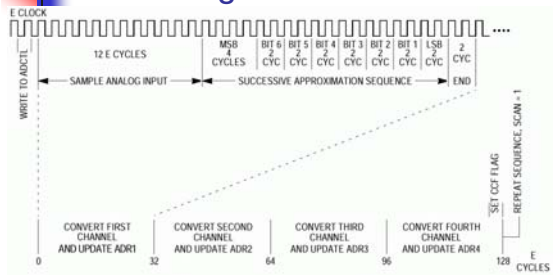


Figure 12-5. Timing Diagram for a Sequence of Four A/D Conversions

M68HC11 — Rev. 5 Reference Manual

A/D pin model

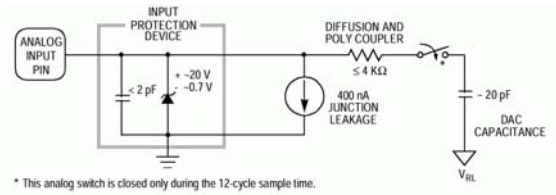


Figure 12-7. Electrical Model of an A/D Input Pin (Sample Mode)

M68HC11 — Rev. 5 Reference Manual

11