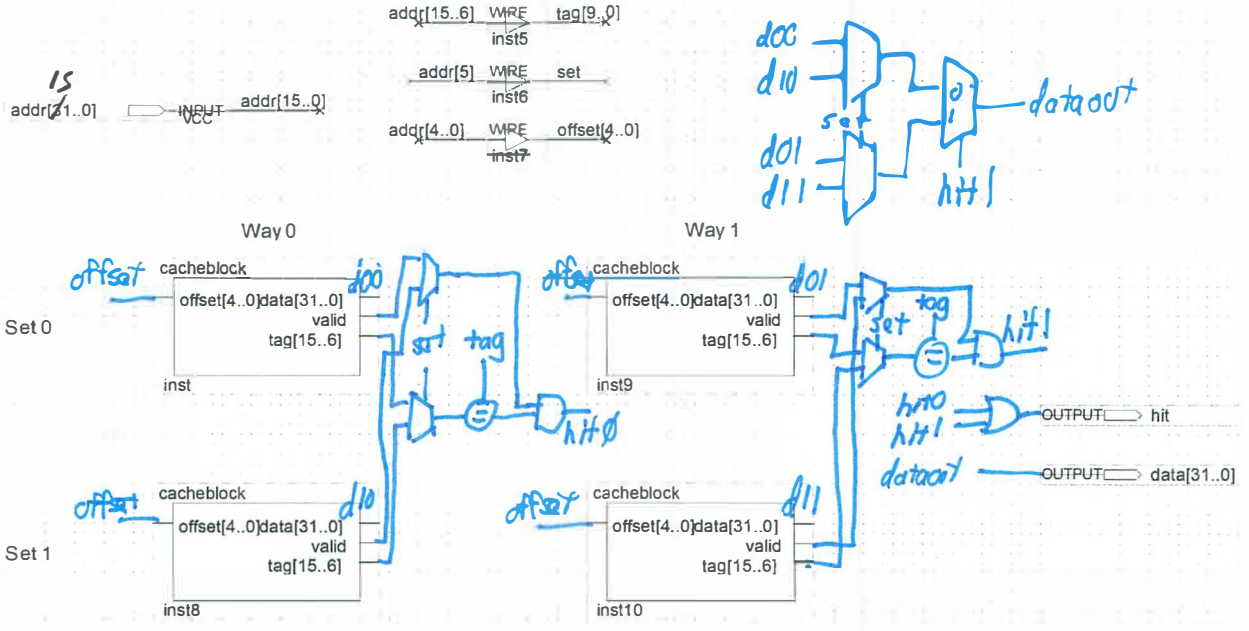
Name Answers

CE-1921 – Dr. Durant – Quiz 10
Spring 2018, Week 10

A partially implemented 2-way cache is shown below. Note that the initial design, which you need to complete, only needs to indicate whether there was a hit and, if there was, output the correct 4-byte value starting from the given address. Assume addresses are word-aligned (multiples of 4). This initial design is severely limited in that it cannot (a) load missed values from main memory or (b) handle writes to memory. Note that the WIRE components provide the correct tag, set, and offset.



For questions 1-3, show your work and give answers in the most appropriate units from kB, MB, GB.

1. (2 points) What is the maximum memory size that this cache can access? 2^{16} (addr. bits) $= 65,536\ B = 64\ kB$
2. (2 points) What is the block size of this cache? 2^5 (offset bits) $= 32\ B$
3. (2 points) What is the total capacity of this cache? $C = \text{blocks} \times \text{blocksize} = \text{sets} \times \text{ways} \times \text{blocksize} = 2 \times 2 \times 32\ B = 128\ B$
4. (4 points) Complete the initial design described above. You may use any standard combinational components including equality comparators, multiplexors, and AND gates.