Name _____Answers_____

CE-1921 – Dr. Durant – Quiz 7
Spring 2018, Week 7

For the pipelined architecture discussed in class…

1. (3 points) Write a sequence of assembly instructions that generates a read-after-write data hazard.
2. (3 points) Describe the preferred (fastest execution) solution to the data hazard that ensures that the processor executes the above sequence properly. ⊖, if stalling
3. (4 points) Draw a pipeline in-flight diagram for your instructions, illustrating key details (e.g., stalling, flushing, and/or forwarding) of how the hazard is resolved. Recall that this diagram shows instructions from top to bottom advancing through the pipeline in time from left to right.

① add r0, r1, #7
    sub r2, r0, r3
    adds r4, r0, r0

There are simpler solutions w/ 1 RAW hazard. This demonstrates hazards on all 3 reads of r0.

② Forwarding. The r0 result exists in the processor by the time it is needed by the ALU in EX for sub & adds. It just has not been written back (WB) yet.

③ add r0, r1, #7
    sub r2, r0, r3
    adds r4, r0, r0
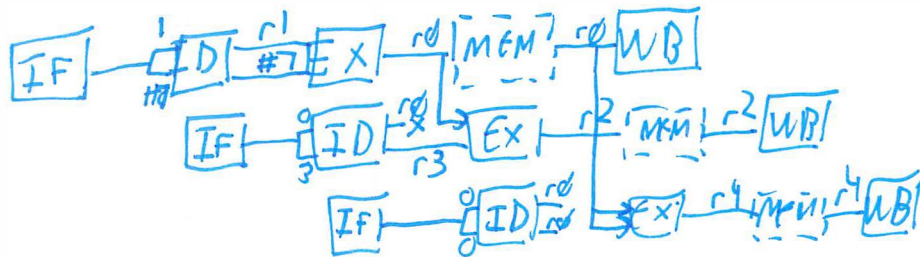
↑ FWD   ↑ 2x FWD

(-½) FWD from post time/
    eg. ALU

ACCEPT:
load -use, correctly