Name Answers

CE-1921-11 – Dr. Durant – Quiz 7
Spring 2016, Week 7

1. (2 points) Describe the fundamental difference between a single-cycle and a multi-cycle processor.
2. (2 points) State the purpose of the instruction register in the multi-cycle processor.
3. (2 points) List, in order, the controller states for the STR instruction on the multi-cycle processor
4. (2 points) What work, if any, is the ALU doing in the 3rd state you listed above?
5. (2 points) For the multi-cycle processor designed in your book (and in lecture), neglecting the speedup of conditional instructions, calculate the average CPI for a program that consists of 70% data processing instructions, 10% load instructions, 10% store instructions, and 10% branch instructions. Show your work.

(1) An MCP takes multiple cycles per instruction but has a shorter cycle time since there is less work to do each cycle.

(2) It holds the machine language instruction throughout the entire execution of that instruction, even when the memory output changes.

(3) fetch → decode → execute → memory write

(4) calculating the address in memory to write to

(5)

	cycles	frequency	contribution to weighted CPI
DP	4	70%	2.8
LDR	5	10%	.5
STR	4	10%	.4
B	3	10%	.3
			4 = average CPI

Name Answers

CE-1921-12 – Dr. Durant – Quiz 7
Spring 2016, Week 7

1. (2 points) Describe the fundamental difference between a single-cycle and a multi-cycle processor.
2. (2 points) State the purpose of the data register in the multi-cycle processor.
3. (2 points) List, in order, the controller states for the LDR instruction on the multi-cycle processor
4. (2 points) What work, if any, is the ALU doing in the 3rd state you listed above?
5. (2 points) For the multi-cycle processor designed in your book (and in lecture), neglecting the speedup of conditional instructions, calculate the average CPI for a program that consists of 50% data processing instructions, 20% load instructions, 10% store instructions, and 20% branch instructions. Show your work.

(1) an MCP takes multiple cycles per instruction but has a shorter cycle time since there is less work to do each cycle.

(2) Hold the memory output for use on the next cycle. Specifically, it is useful when it contains the value read from memory in LDR. Memory read & reg write happen on separate cycles to keep cycle time short.

(3) fetch → decode → execute → memory read → register writeback

(4) calculating the address in memory to read from

(5)

	cycles	Frequency	contribution to weighted avg.
DP	4	50%	2
LDR	5	20%	1
STR	4	10%	.4
B	3	20%	.6

4 = average CPI