CE-1921 – Dr. Durant – Quiz 6
Spring 2020, Week 8

Open: book, notes, assembler/disassembler, previous quizzes, Internet. But, do not discuss the quiz with anyone except the professor until after everybody's work is submitted and the due date has passed. Please submit in Teams Assignments.

The following instructions are executing in the pipelined processor from Figure 7.46 of the book. The instructions are arranged to avoid data hazards.

```
                          @ Machine    clock:
                          @ code        1   2   3   4   5
ldr r0, [r1, #0x40]       @ 0xE5910040 IF  ID  EX  MEM WB
add r1, r1, #0x200        @ 0xE2811C02     IF  ID  EX  mem
sub r3, r2, #0xC0         @ 0xE24230C0         IF  ID  EX
eor r4, r0, #0xA5         @ 0xE22040A5             IF  ID
orr r1, r1, #0x00C00000 @ 0xE3811503                 IF
```

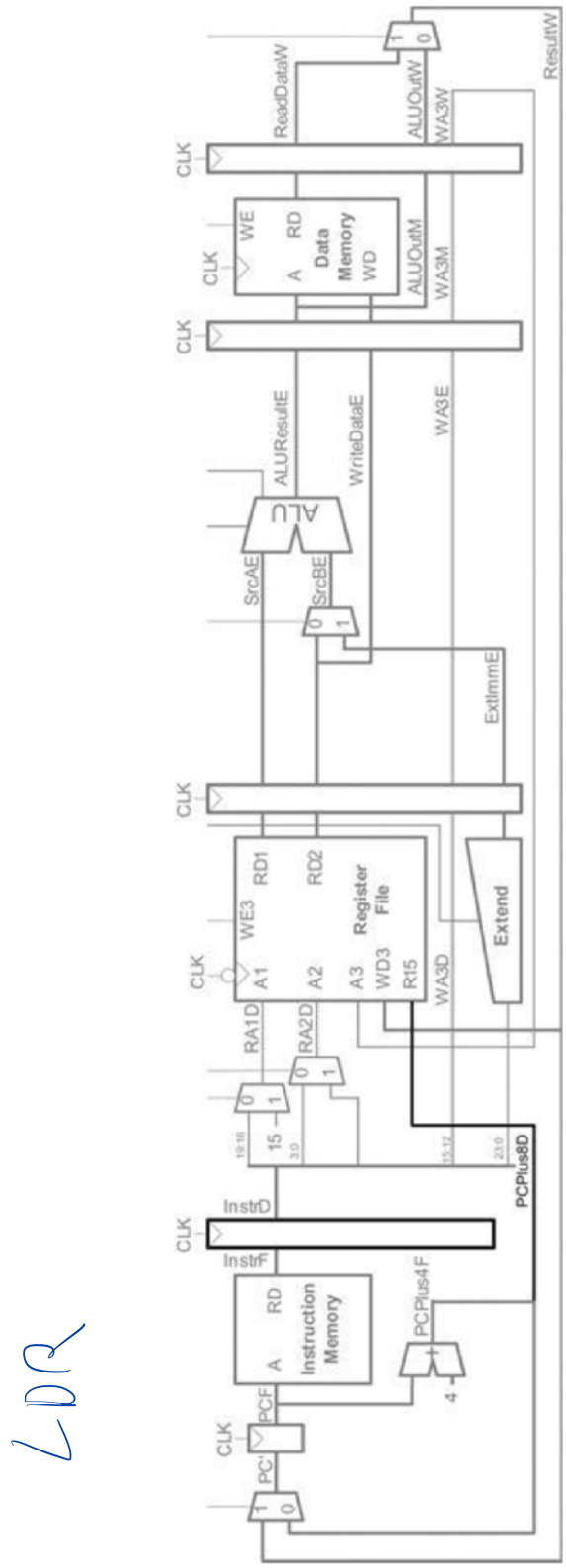
Discussion of program

- At the start, r1 contains 0x00300000, which is a memory address inside a large data structure.
- ldr loads from memory address 0x00300040. Assume the value in memory is 0xB300002F.
- add modifies r1 to reference a location later in the data structure
- sub takes the value in r2 (assume it's 0x000000F3), subtracts #0xC0, and writes the result to r3.
- eor takes the value that was loaded into r0 (0xB300002F) and toggles 4 bits per the immediate value #0xA5. The result will be written to r4.
- Finally, the orr instruction takes r1, which the add instruction changed to 0x00300200, and turns on 2 bits per the mask #0x00C00000 to calculate the address of a new location within the data structure.

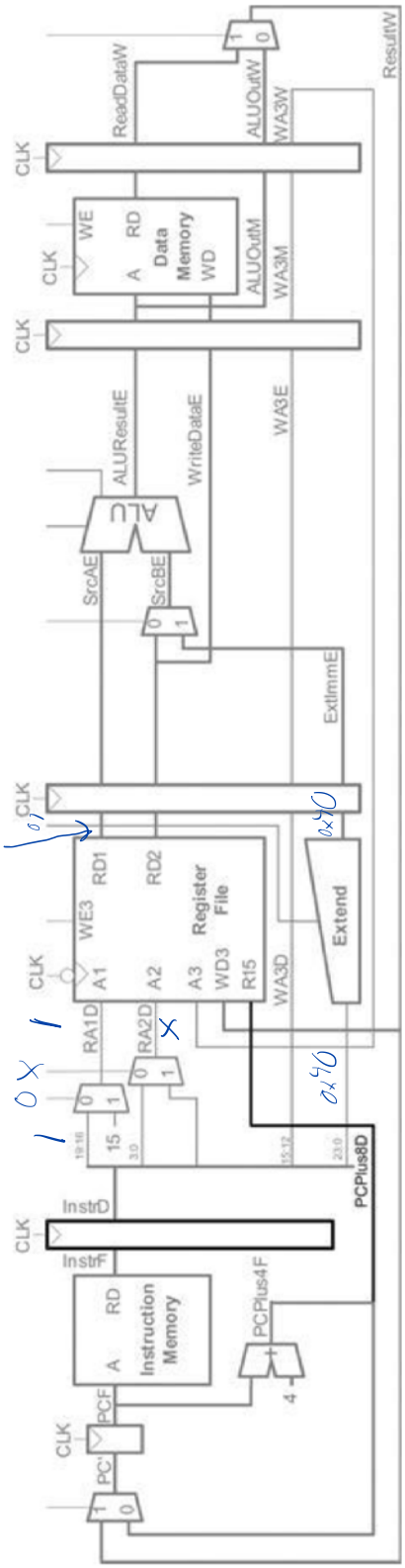
Your task

- Mark up the 5 copies of the processor showing these instructions moving through the pipeline.
- Show all relevant control and data path values. You do not need to show what the PC is doing, but you should show InstF (fetched instruction), etc.
- Control signals are all active high.
- Mark the ALU control with an operation name (sub, or, passB, etc.).
- Write the instruction above the appropriate stage of the pipeline. Thus, in cycle 3, IF (instruction memory stage) will be labeled SUB; ID (register file stage) will be labeled ADD, and EX (ALU stage) will be labeled LDR.
- Assume the pipeline was empty before these instructions began; thus in cycle 3 you will show no signals for MEM and WB and this will be understood to mean that neither the data memory nor the register file is being written to; you can mark the signals 0 for inactive if you prefer.
- Some signals will be X for don't care. For example, when there is no SRC2 register for an instruction, you should show the select input into the A2 MUX in the decode stage as X and thus RA2D=A2 would also be X.

Clock Cycle 1



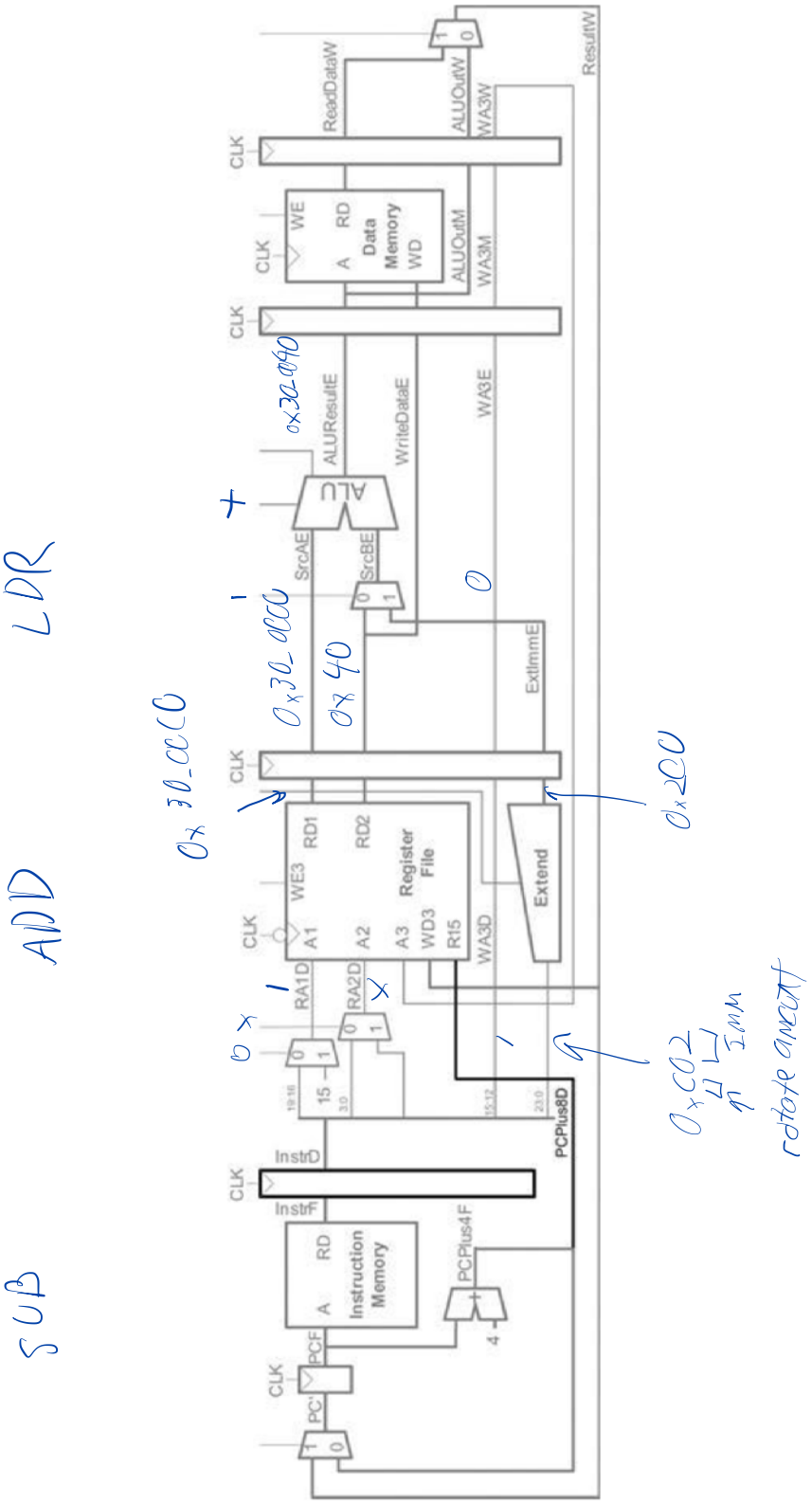
Clock Cycle 2



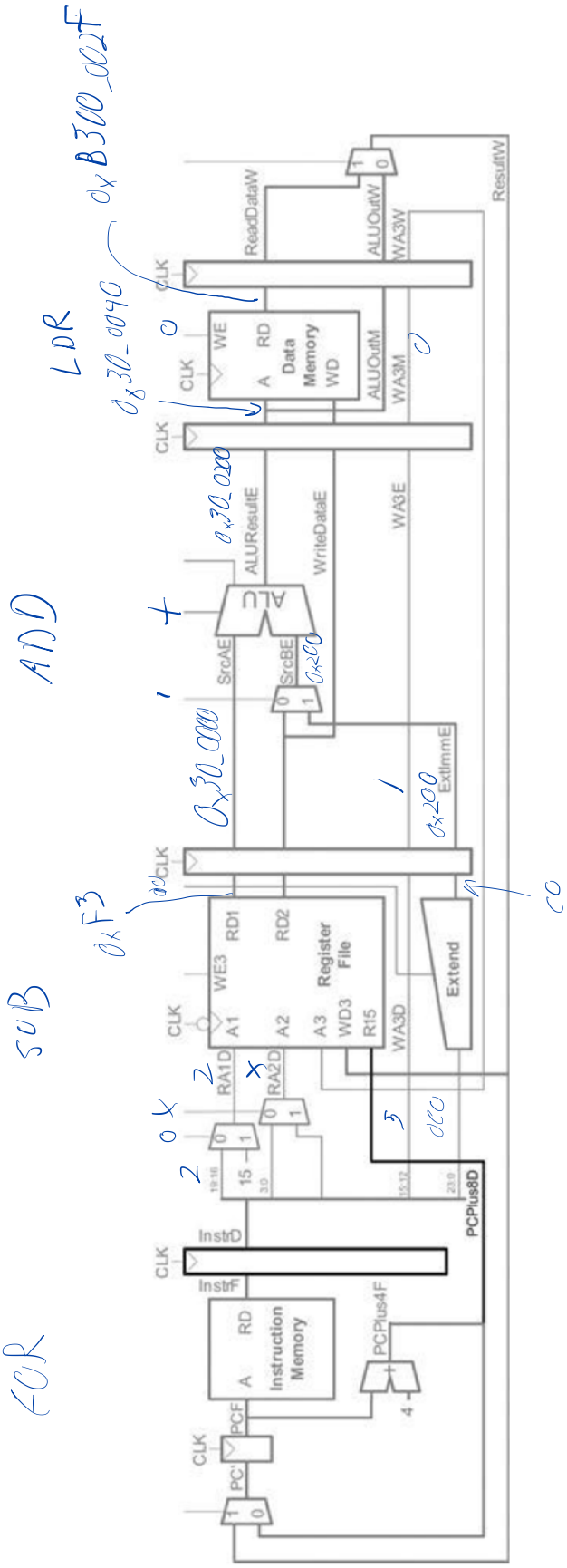
LDR

ADD

Clock Cycle 3



Clock Cycle 4



Clock Cycle 5