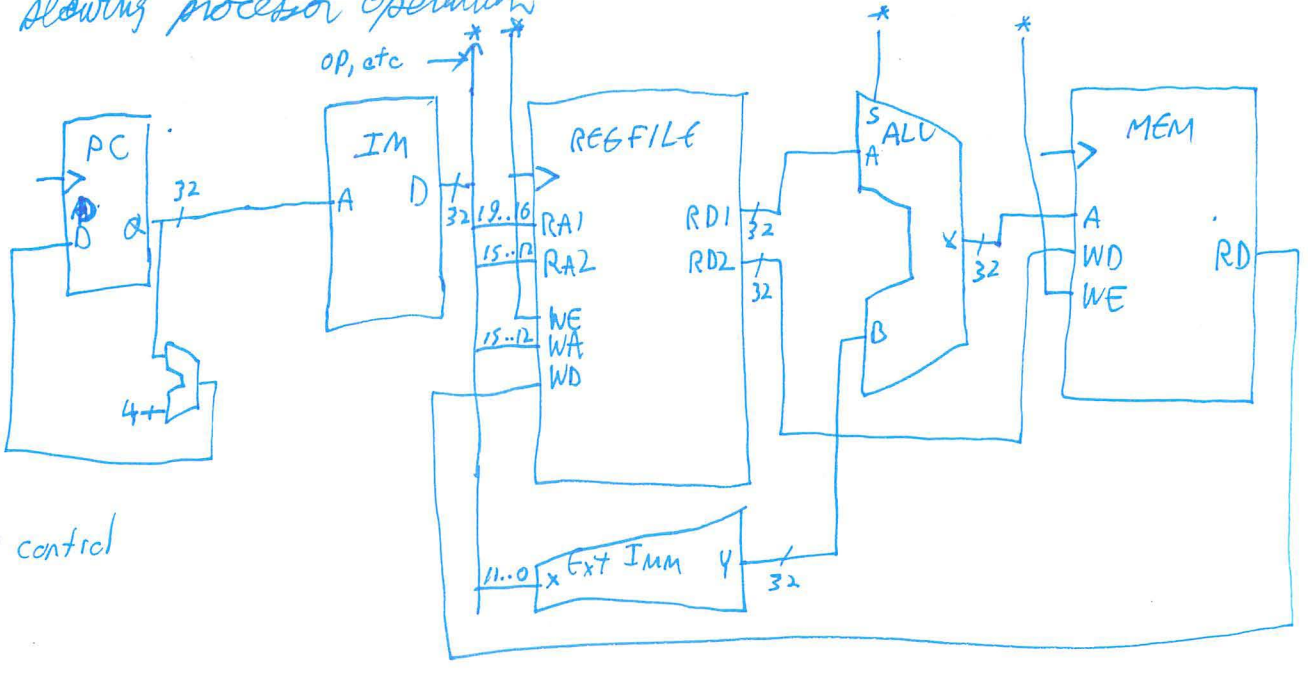
Name Answers

CE-1921-11 – Dr. Durant – Quiz 5
Spring 2016, Week 5

1. (1 point) Define the Princeton bottleneck.
2. (5 points) Draw the ARM single-cycle processor designed in lecture that can execute (just) `ldr` and `str` using (just) (positive) register offset (e.g., "`[r6,#8]`") addressing mode.
3. (2 points) List all the control signals for your processor above and indicate what their values must be when executing `str r9,[r4,#20]`.
4. (2 points) State the execution time equation. Remember that time is the product of three terms.

(1) When there is a single memory for both instructions & data it must complete 2 operations on a load/store operation, slowing processor operation

(2)



*: control

(3) RegWrite = 0
AluOp = ADD
MemWrite = 1

(4) time = CPI × instruction count × clock period
clocks/instr. IC T

Name Answers

CE-1921-12 – Dr. Durant – Quiz 5
Spring 2016, Week 5

1. (5 points) Draw the ARM single-cycle processor designed in lecture that can execute (just) `ldr` and `str` using (just) (positive) register offset (e.g., "`[r6,#8]`") addressing mode.
2. (2 points) List all the control signals for your processor above and indicate what their values must be when executing `ldr r7,[r3,#64]`.
3. (1 point) Explain why `ldr` has the longest delay of any instruction in the single-cycle processor.
4. (2 points) State the execution time equation. Remember that time is the product of three terms.

(1) attached

(2) RegWrite = 1
AluOp = ADD
MemWrite = 0

(3) Longest propagation path: PC → IM → REGFILE → ALU → MEM → REGFILE

read address — add offset — str stops here — write result back to regfile

(4) time = IC × CPI × T

IC: instruction count
CPI: clocks / instruction
T: clock period