Name Answers

CE-1921 – Dr. Durant – Quiz 4
Spring 2018, Week 4

1. (5 points) Assemble the following instruction to ARMv4 machine code: **`subne r3,r4,#0x5a`**
   a. Label and box in each field above the boxes below. "cond" has been done for you.
   b. Box in and fill each field in the next row with the value for that field.
   c. Convert values to binary in the following row.
   d. Convert values to hexadecimal in the final row.

	31 30 29 28	27 26	25	24 23 22 21	20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4 3 2 1 0
a	cond	OP	I	opcode	S	R_n	Rd	rotate	immed_8
b	NE	DP	1	SUB	0	4	3	0	0x5A
c	0 0 0 1	0 0	1	0 0 1 0	0	0 1 0 0	0 0 1 1	0 0 0 0	0 1 0 1 1 0 1 0
d	1	2		4		4	3	0	5 A

2. (5 points) Assemble the following instruction to ARMv4 machine code: **`str r5,[r7],#-0x20`**

	31 30 29 28	27 26	25	24	23	22	21	20	19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
a	cond	OP	$\overline{I}$	P	U	B	W	L	R_n	Rd	Imm
b	AL	LD/ST	0	0	SUB	0 (word/byte)	0	0 (store/load)	7	5	0x020
c	1 1 1 0	0 1	0	0	0	0	0	0	0 1 1 1	0 1 0 1	0 0 0 0 0 0 1 0 0 0 0 0
d	E	4		0		7		5	0	2	0

Post-index ∴ PW=00 "unsigned"
Subtract offset ∴ U=0
Store word ∴ LB=00 (load byte)

Rd gets data for load/store
Makes sense since Operand1, Operand2 go to ALU
regularity
R_n
Imm_{12}

subne r3,r4,#0x5a
str r5,[r7],#-0x20

ARM ARM (thumb) AArch64 Mips (32) Mips (64) PowerPC (32) PowerPC (64)
Sparc x86 (16) x86 (32) x86 (64)

Assemble

Assembly

```
Little endian:

"\x5a\x30\x44\x12\x20\x50\x07\xe4"

Big endian:

"\x12\x44\x30\x5a\xe4\x07\x50\x20"
```

"\x12\x44\x30\x5a\xe4\x07\x50\x20"

◉ ARM ○ ARM (thumb) ○ AArch64 ○ Mips (32) ○ Mips (64) ○ PowerPC (32) ○ PowerPC (64)
○ Sparc ○ x86 (16) ○ x86 (32) ○ x86 (64)

○ Little Endian ◉ Big Endian

Disassemble

Disassembly

```
0x00000000: subne r3, r4, #0x5a
0x00000004: str r5, [r7], #-0x20
```