Name Answer

CE-1921-11 – Dr. Durant – Quiz 4
Spring 2017, Week 4

1. (5 points) Assemble the following instruction to ARMv4 machine code: **`adds r3,r6,r7`**
   a. Label and box in each field above the boxes below. "cond" has been done for you.
   b. Box in and fill each field in the next row with the value for that field.
   c. Convert values to binary in the following row.
   d. Convert values to hexadecimal in the final row.

	31 30 29 28	27 26	25	24 23 22 21	20	19 18 17 16	15 14 13 12	11 10 9 8 7	6 5	4	3 2 1 0
a	cond	op	I	opcode	S	Rn	Rd	shamt	sh	0	Rm
b	always	0	0	0 1 0 0 (4)	1	6	3	0	0 (LSL)	0	7
c	1 1 1 0	0 0	0	0 1 0 0	1	0 1 1 0	0 0 1 1	0 0 0 0 0	0 0	0	0 1 1 1
d	E	0		9		6	3	0	0		7

No deduction for reg shift, if "rg" → 0x E0963017 (but, it's wrong, can't guarantee Rx=0)
(-1/4) S=0
(-1/2) reg sh. w/ other/partial errors

2. (5 points) Assemble the following instruction to ARMv4 machine code: **`ldreq r4,[r3,#0x20]!`**

	31 30 29 28	27 26	25	24	23	22	21	20	19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
a	cond	OP	I	P	U	B	W	L	Rn	Rd	Imm
b	equal	0 1	0	1	1	0	1	1	3	4	0x20
c	0 0 0 0	0 1	0	1	1	0	1	1	0 0 1 1	0 1 0 0	0 0 0 0 0 0 1 0 0 0 0
d	0	5		B		3			4	0	2 0

(-1/4) 20_{10} vs 20_{16} (-1/2) Wrong Operand2/partial
(-1/2) PW≠11
(-1/2) Reg Offset
(-1/4) I=1

Name Answers

CE-1921-21 – Dr. Durant – Quiz 4
Spring 2017, Week 4

1. (5 points) Assemble the following instruction to ARMv4 machine code: `orrne r2,r9,#0xC5`
   a. Label and box in each field above the boxes below. "cond" has been done for you.
   b. Box in and fill each field in the next row with the value for that field.
   c. Convert values to binary in the following row.
   d. Convert values to hexadecimal in the final row.

	31 30 29 28	27 26	25	24 23 22 21	20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4 3 2 1 0
a	cond	op	I	opcode	S	Rn	Rd	rotate	Immediate
b	not equal	0	1	0 0 0 (CC)	0	9	2	0	0xC5
c	0 0 0 1	0 0	1	1 0 0 0	0	1 0 0 1	0 0 1 0	0 0 0 0	1 1 0 0 0 1 0 1
d	1	3		8		9	2	0	C 5

2. (5 points) Assemble the following instruction to ARMv4 machine code: `str r2,[r6],#-8`

	31 30 29 28	27 26	25	24	23	22	21	20	19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
a	cond	op	I	P	U	B	W	L	Rn	Rd	Imm
b	always	01	0	0	0	0	0	0	6	2	8
c	1 1 1 0	0 1	0	0	0	0	0	0	0 1 1 0	0 0 1 0	0 0 0 0 0 0 0 0 1 0 0 0
d	E	4		0		8			6	2	0 0 8

(-1/4) Rn ≠ Rd
(-1/4) IMM SIGNED 0xF8 (& (-1/4) if U≠0)
(-1/2) PW≠00 (post-inc)
(-1/2) cond AL