Name ___ANSWERS____

CE-1921-11 – Dr. Durant – Quiz 2
Spring 2017, Week 2

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1. (1 point) Explain how the assembler handles mov r0,#-5 even though ARM immediates are unsigned. Hint: look at the arithmetic instructions below mov.
2. (1 point) State the maximum memory size allowed by the ARM architecture.
3. (2 points) The 32-bit word 0xF005BA11 is stored at 0x1400. What byte is stored 0x1401?
4. (2 points) R5 contains 0xA5A55A5A, R6 contains 0x1200, and R7 contains 0x80. Describe ***all*** register and memory values that change as a result of executing LDR R5,[R6,R7]!.
5. (2 points) State the instruction that determines the values of all the ARM condition flags in preparation for evaluating any relational operation between R1 and R2.
6. (2 points) Give an example of a conditional branch instruction and describe what exactly it does.

Answers

1. It uses the mvn, which moves the notted version of the immediate. Specifically, it actually assembles mvn r0,#4. Note that the immediate is 4, not 5, because the instruction merely inverts all the bits (part of the 2's complement operation). It doesn't add 1 as 2's complement requires.
2. The address bus is 32 bits wide and is used to address bytes (not 32-bit words). Thus there are 2^32 bytes or 4 GB in the ARM memory space; this is the maximum memory allowed.
3. 0xBA is stored at address 0x1401. ARM prefers little endian, so the LS byte is stored first (at the lowest address).
4. We're loading using pre-increment addressing mode, which means that the base register will be modified before it is used to address memory.
    a. R6 += R7, so R6 becomes 0x1280
    b. R5 gets overwritten with whatever value is stored at 0x1280 – 0x1283 in little endian order. That is, the data at 0x1280 goes into the LS byte of R5, while the data at 0x1283 goes into the MS byte of R5.
5. cmp r1, r2
6. blo L57 ; branches to line with label L57 if the result of the last comparison was that the first operand was lower than the second one. Lower means that the operands are to be interpreted as unsigned. ("Less than" is the signed version of the unsigned "lower.")
7.

Name ____ANSWERS____

CE-1921-21 – Dr. Durant – Quiz 2
Spring 2017, Week 2

1. (1 point) State the range of immediate widths on ARM.
2. (1 point) Describe how position in the modern memory pyramid implies speed and capacity.
3. (2 points) The 32-bit word 0xBA11A575 is stored at 0x1400. What byte is stored 0x1402?
4. (2 points) R5 contains 0xA5A55A5A, R6 contains 0x1200, and R7 contains 0x80. Describe ***all*** register and memory values that change as a result of executing STR R5,[R6],R7.
5. (2 points) List and briefly describe the 4 ARM condition flags.
6. (2 points) Give an example of an arithmetic instruction that writes its result to the destination register only if the previous compare operation compared two unsigned numbers, finding the first to be larger.

Answers

1. 8-12 bits. This can be found on the ARM instruction format card; the "data processing immediate" format instruction has an 8-bit immediate (plus a 4-bit rotate field), while the "load/store immediate offset" instruction has a 12-bit immediate.
2. Fast memory is kept closer to the top of the pyramid (closer to the CPU), but this memory is expensive, so its capacity is limited.
3. 0x11 is stored at address 0x1402. ARM prefers little endian, so the LS byte is stored first (at the lowest address).
4. We are storing using post-increment addressing mode, which means the base address register will be modified, but the value before modification is used to address memory.
    a. Memory 0x1200 gets the value 0xA5A55A5A
    b. R6 gets incremented by R7's value, becoming 0x1280. Note that R6 was used to address memory before this update.
5. NZCV
    a. Negative – whether the 1st bit is on, 2's complement interpretation
    b. Zero – whether all bits in the result are 0
    c. Carry – whether there was a carry out
    d. oVerflow – whether there was a signed (2's complement) overflow
6. cmp r0,r1
   movhi r2,#0xAB