Name Answers

CE-1921-11 – Dr. Durant – Quiz 2
Spring 2016, Week 2

1. (1 point) State the range of immediate widths on ARM.
2. (1 point) State the maximum memory size allowed by the ARM architecture.
3. (2 points) The 32-bit word 0xacce55ed is stored at 0x1400. What byte is stored 0x1401?
4. (2 points) R5 contains 0xA5A55A5A, R6 contains 0x1200, and R7 contains 0x80. Describe ***all*** register and memory values that change as a result of executing STR R5,[R6,R7]!.
5. (2 points) State the instruction that sets/clears all the ARM condition flags in preparation for evaluating any relational operation between R1 and R2.
6. (2 points) Give an example of an arithmetic instruction that writes its result to the destination register only if the previous compare operation compared two unequal numbers.

① 8-12 (a 24 if you count SWI) (-¼ 8 only)

② 2^{32} B = 4 GB (-¼ if address width only)

③ 0x55 (little endian) -½ for CE (endian wrong)

④ (a) pre-increment : R6 += R7 R6 0x1280 as 32-bit value

(b) memory @ 0x1280-3 changes to 0x A5A55A5A
byte @ 0x1283 byte @ 0x1280

(c) PC increases by 4

⑤ CMP R1, R2

⑥ SUBNE R6, R0, R1
↑ not equal

Name Answers

CE-1921-12 – Dr. Durant – Quiz 2
Spring 2016, Week 2

1. (1 point) State the range of immediate widths on ARM.
2. (1 point) Describe how position in the modern memory pyramid implies speed and size.
3. (2 points) The 32-bit word 0x50f7ba11 is stored at 0x1400. What byte is stored 0x1402?
4. (2 points) R5 contains 0xA5A55A5A, R6 contains 0x1200, and R7 contains 0x80. Describe ***all*** register and memory values that change as a result of executing LDR R5,[R6],R7.
5. (2 points) List and briefly describe the 4 ARM condition flags.
6. (2 points) Give an example of a conditional branch instruction and describe what exactly it does.

(1) 8-12

(2) top = small, fast, expensive (e.g., SRAM registers)
bottom = huge, slower, cheap (e.g., hard disk)

(3) 0xF7 (little endian)

(4) (a) R5 gets a value from memory, R6 is the memory address
(b) R6 += R7 ← prepare to access other data
(c) PC += 4

(5) N negative
V ~~zero~~ signed overflow
Z zero
C carry

(6) BHS L0
HS = higher or same, unsigned a ≥ b (from CMP Ra, Rb)
goes to L0 (next PC) if a ≥ b
goes to next instruction otherwise