MSOE EECS Department – Dr. Durant
CE1921: Wk. 9 Lab Grading Checklist

Name: _____

Item	**Score**
All BDFs shown in report: fetch, decode, execute, top level	/ 20
Other VHDL supporting files that are new this week (pc, constant{4,8}, adder) shown in report	/ 10
RTL. The RTL view shows the hardware built based on your VHDL. It is often the easiest way to spot missing connections and hardware that you didn't intend to be created. Open and zoom in on key areas of this large diagram (including decode and execute), showing your RTL in multiple segments as needed for clarity. Include a brief description noting whether the rendered hardware is what you expected.	/ 20
QAR (Quartus Archive) emailed as separate file	/ 10
Complete simulation. See "Simulation Requirements" in the lab specification.	/ 15
Simulation documentation. For all CE1921 simulations explain why your simulation indicates correct behavior by drawing on your simulation or adding text explanations to convince a reader your results are correct.	/ 25
Total	/ 100

- Email your PDF and other file(s) with a subject such as CE1921 Lab Submission.
  - PDF: Print all your materials (items above) to PDF and add this as the first page. Arrange everything in the ***order*** listed above.
    - For the simulation (especially) you may get the best results by taking a screen shot (Alt + Print Screen; on some laptop keyboards you need to also press the fn key to access Print Screen (e.g., on my keyboard fn+rightShift is Print Screen, so I need to press 3 keys)). Then crop it accordingly, perhaps with Windows 10 Paint, although I prefer the free IrfanView program.
  - QAR (Quartus Archive): does not need to be shown in your PDF
- This is due by the end of the week during which it is assigned.