

# MSOE EECS Department – Dr. Durant

## CE1921: Wk. 6 Lab Grading Checklist

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Name: \_\_\_\_\_

Item	Score
from VHDL. <b>Disassemble</b> the entire program and show it as comments as is already done for 3 instructions. You should check your work with either or both of (a) an online disassembler and (b) an assembler to confirm you get the given machine code back.	/ 40
from RTL. The RTL view shows the hardware built based on your VHDL code. It is often the easiest way to spot missing connections and hardware that you didn't intend to be created.	/ 10
from simulation. See "Simulation Requirements" in the lab specification.	/ 10
from simulation documentation. For all CE1921 simulations explain why your simulation indicates correct behavior by annotating your simulation sufficiently to convince a reader your results are correct. You can draw on your simulation and/or add text explanations.	/ 40
<b>Total</b>	/ 100

- Email your PDF and VHDL file to the instructor with a subject such as CE1921 Lab Submission.
  - PDF: Print all your materials (items above) to PDF and add this as the first page. Arrange everything in the **order** listed above.
    - For the simulation (especially) you may get the best results by taking a screen shot (Alt + Print Screen; on some laptop keyboards you need to also press the fn key to access Print Screen (e.g., on my keyboard fn+rightShift is Print Screen, so I need to press 3 keys)). Then crop it accordingly, perhaps with Windows 10 Paint, although I prefer the free IrfanView program.
  - VHDL: Also include your .VHDL file itself.
- This is due by the end of the week during which it is assigned.