MSOE EECS Department – Dr. Durant
CE1921: Wk. 5 Lab Grading Checklist

Name: _____

Item	**Score**
regfile VHDL (2 read ports, 1 write port, sync. reset). Document with comments; see example in lab for appropriate level of information, but the format doesn't have to exactly match.	/ 30
regfile RTL. The RTL view shows the hardware built based on your VHDL code. It is often the easiest way to spot missing connections and hardware that you didn't intend to be created.	/ 10
regfile simulation. See "Simulation Requirements" in the lab specification. Most of your simulations should show a successful write (that is, a value written to a register is later read out on RD1/RD2).	/ 30
regfile simulation documentation. For all CE1921 simulations explain why your simulation indicates correct behavior by annotating your simulation sufficiently to convince a reader your results are correct. You can draw on your simulation and/or add text explanations.	/ 30
Total	/ 100

- Email your PDF and VHDL file to the instructor with a subject such as CE1921 Lab Submission.
  - PDF: Print all your materials (items above) to PDF and add this as the first page. Arrange everything in the ***order*** listed above. You are welcome to use any PDF editing software. If what is available on your MSOE laptop (e.g., Acrobat) turns out to lack any needed features (e.g., combining pages), please mention it in the teams channel and we will figure out an alternative.
    - For the simulation (especially) you may get the best results by taking a screen shot (Alt + Print Screen; on some laptop keyboards you need to also press the fn key to access Print Screen (e.g., on my keyboard fn+rightShift is Print Screen, so I need to press 3 keys)). Then crop it accordingly, perhaps with Windows 10 Paint, although I prefer the free IrfanView program.
  - VHDL: Also include your .VHDL file itself.
- This is due by the end of the week during which it is assigned.