Milwaukee School of Engineering
CE1921 Computer Architecture
Dr. Durant

Final Exam

May, 2017

Name: _____

Read all questions carefully – some have multiple parts.

Please ask if any questions are not clear.

Allowed materials: Dr. Durant's reference card

Good luck!

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1. (5 points) Describe 2 situations in which the CPI of a pipelined processor falls below its ideal value.
2. (5 points) State both an advantage and a disadvantage of a multicycle processor compared with a single-cycle processor, assuming that both are made of similar functional blocks (ALUs, REGFILE, etc.)?
3. (10 points) Convert from assembly to machine language: orrne r9,r4,r13

4. (10 points) Convert from machine to assembly language: 0x05164008
5. (5 points) Following conventional ARMv4 register usage, which registers must be used for the arguments and return value for the function int pow(int x, int y)?

6. (20 points) Draw a block diagram for a single-cycle processor that supports data processing instructions (at least where operand2 can be either an immediate or a register value), load/store with offset addressing, and branches (at least unconditional without link). Include the necessary MUXes and major components such as the register file and ALU.

7. (10 points) Draw the state diagram for an MCP controller that implements data processing, ldr, str, and b instructions. You do NOT need to include outputs, just meaningful state names and transition criteria.
8. (5 points) What is the CPI for the MCP you just drew given an instruction mix of 10% ldr, 15% str, 65% data processing, 10% branch?

9. (10 points) Write an instruction sequence where one data processing instruction simultaneously causes two data hazards. Also sketch the pipeline in-flight diagram for proper handling of the hazards, illustrating any necessary stalls, flushes, and forwards.
10. (10 points) Consider the instruction ldr pc,[r8,#4]. Describe two potential hazards with this instruction and discuss a strategy for solving both.

11. (5 points) Describe a memory usage pattern in which a write-back cache has a performance advantage over a write-through cache.
12. (5 points) For a 4096 B cache that has 128 blocks and is 4-way set associative, show how a 32 b memory address breaks down into offset, tag, and set/index fields.