Milwaukee School of Engineering
CE2930 Introduction to Computer Architecture
Dr. Durant

Final Exam

Tuesday, May 19, 2009

Name: _____

Read all questions carefully – some have multiple parts.

Please ask if any questions are not clear.

Good luck!

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1. (3 points) State the standard execution time equation for a program.
2. (12 points) Draw a block diagram for MIPS single cycle processor. Include the necessary MUXes, and major components such as the register file and ALU.
3. (4 points) In general, what is the longest running instruction on the SCP? Explain why this is the case.

4. (4 points) If sw instructions take 800 ps on the SCP, what can you say about the maximum operating frequency of the processor? Hint: what additional information would allow you to calculate the maximum frequency fairly accurately?
5. (6 points) Convert from assembly to machine language: nor $t9, $at, $a2
6. (6 points) Convert from machine to assembly language: 0x8C2F29BA

7. (5 points) Discuss how you could modify the SCP to implement a BHI instruction (branch if higher [unsigned]).
8. (6 points) Discuss the similarities and differences in calculating the cycle time for the SCP and the MCP given subblock and component speeds.
9. (6 points) Draw the state diagram for the controller for the MCP that implements the mini-core instruction set: add/and/nor/or/sub, R and I (for some) formats as present in MIPS; lw/sw; beq. You do NOT need to include outputs, just meaningful state names and transition criteria.
10. (4 points) What is the CPI for the MCP you just drew given an instruction mix of 20% lw, 5% sw, 45% R-format, 20% I-format, 10% branch?

11. (6 points) Discuss the following statement: "From a simple clock speed perspective, the pipelined processor can be run at a similar rate to the MCP, and these are both much faster than the SCP."
12. (4 points) What hardware would need to be added to your pipelined processor so that it could simultaneously predict a branch was taken and was not taken?
13. (4 points) What are the benefits of storing branch prediction information associated with a particular PC address vs. for all branches of a particular type (e.g., beq)?
14. (5 points) Draw the state diagram and describe the logic behind a branch predictor that has 2 bits of state information.

15. (3 points) What are the 3 types of hazards in a pipelined processor?
16. (4 points) Describe the key benefit of a fully associative cache. Hint: consider the replacement policy.
17. (5 points) Describe the hardware complexity of a fully associative cache re a direct-mapped cache.

18. (3 points) What is the ideal CPI for the pipelined processor you designed in class? Justify your answer.
19. (4 points) How is the CPI affected by branches? Include a discussion of the worst case impact of branches on the CPI.
20. (6 points) How is the CPI affected by cache misses? Discuss how the effect can be minimized.