Milwaukee School of Engineering
CE1910 Digital Logic II: Sequential Systems
Dr. Durant

Final Exam

Monday, May 18, 2009

Name: _____

Read all questions carefully – some have multiple parts.

Please ask if any questions are not clear.

Good luck!

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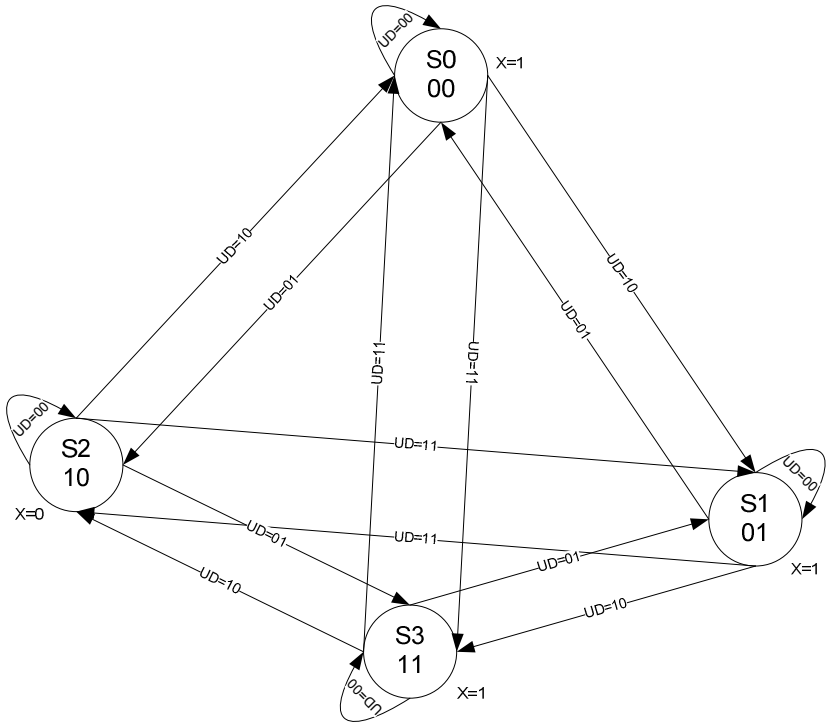
1. (20 points) Complete the following state machine design problem for a vending machine.
    A. (10 points) Draw the complete state diagram, showing all inputs, outputs, and transitions, for a soda vending machine that accepts nickels ($0.05), dimes ($0.10), and quarters ($0.25). The coin acceptor outputs 00 as an input to your state machine when no coins are being inserted and outputs 01 for a nickel, 10 for a dime, and 11 for a quarter for an appropriate amount of time around the next active system clock edge. The vending machine has a single output that goes high for 2 clock cycles when it is time to dispense a soda. Sodas cost $0.50. Extra money is not returned, but is kept towards the next purchase.

B. (10 points) Draw a timing diagram showing behavior of the system from the initial state (0 balance) when the following coins are inserted in order: dime, nickel, quarter, nickel, quarter, dime, quarter. You must illustrate the current state the machine is in at each point in the timing diagram; either method used in class (and Quartus) of doing this is acceptable.

2. (30 points) Consider the following state diagram:



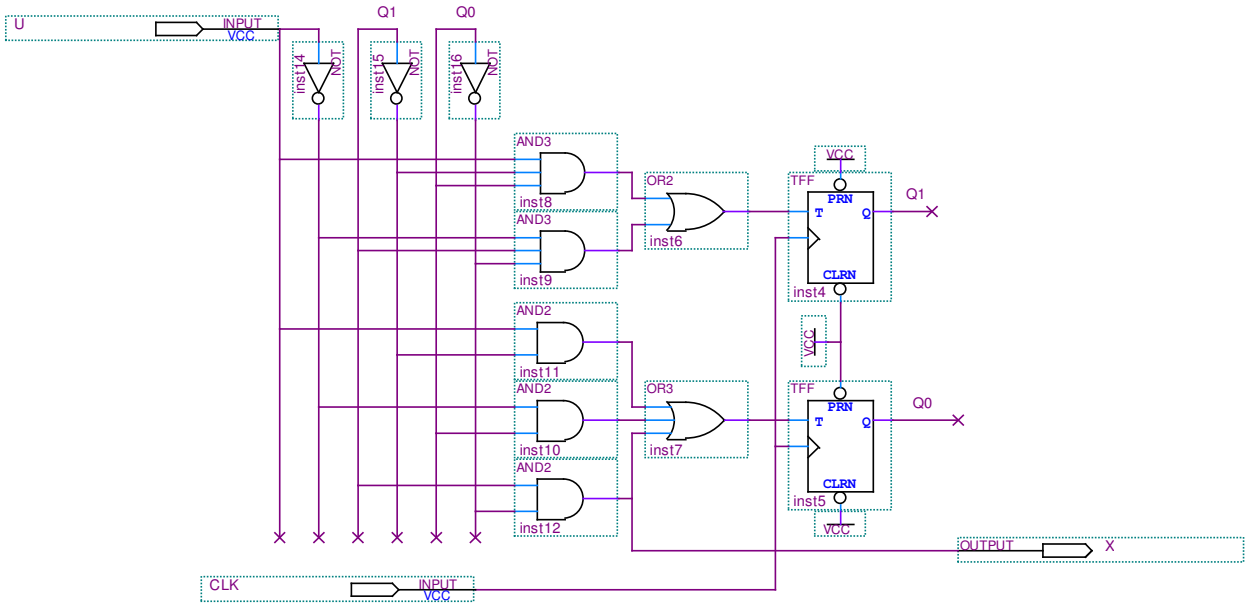
A. (10 points) Draw the design truth table for this FSM, showing both excitation and output values for each combination of current state and input values. Design the excitation table for DFFs.

B. (5 points) Write the ***canonical*** SOP equations for the next state logic and the output logic. You may use one of the abbreviated forms.

C. (10 points) Draw and use K-maps for all the next state and output bits to determine the ***minimum SOP expressions*** for all values.

D. (5 points) Draw the complete circuit that implements this FSM using DFFs and discrete gates. You may use simplified logic if you show how you derived it from the SOP equations above, but SOP logic is acceptable. Use DFFs with both Q and Qn outputs to simplify implementation.

3. (20 points) Consider following FSM.

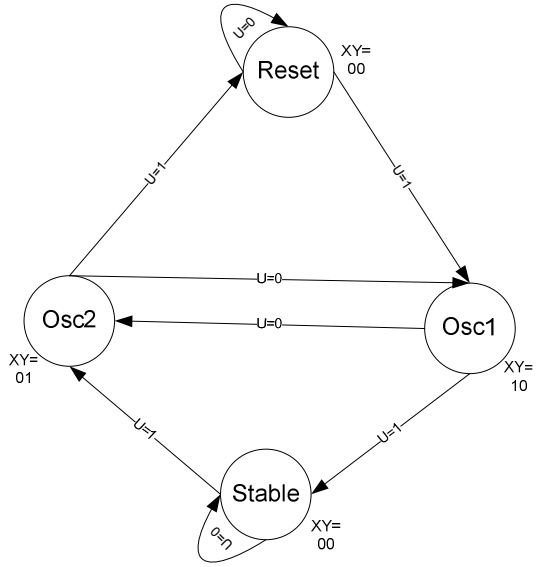


a. (5 points) Derive the **excitation and output equations**. Note that these are ***TFFs***, not DFFs.

b. (10 points) Derive the next state table with outputs.

c. (5 points) Draw the state diagram with inputs and outputs.

4. (20 points) Write the complete VHDL file, including entity and behavioral architecture, implementing the following FSM:



5. (2 points) When does a ***transparent*** register update its stored value?

6. (2 points) **Contrast** combinational and sequential systems.

7. (2 points) What is a ***purpose*** of the RTL viewer in Quartus?

8. (2 points) Briefly describe the operation of a ***ring*** counter.

9. (2 points) Define register file.