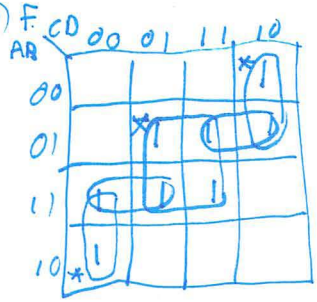
Name Answers

CE-1901-11 – Dr. Durant – Quiz 7
Fall 2016, Week 8 Quiz

1. (4 points) Glitches
   a. ***Derive*** the minimized SOP expression for F(ABCD) = $\Sigma_m(2,5,6,7,8,12,13,15)$.
   b. ***Determine*** between which pair(s) of minterms a (1-bit input change) glitch may occur.
   c. ***Modify*** the expression for F to avoid all glitches.
2. (2 points) ***Write*** the logic equation for the 8:1 MUX, y = f(s,d), where s and d are 0-based vectors of appropriate length. Remember that there is a product term for each of the data terms; this product term checks all values of s to make sure they match the term's corresponding s-minterm.

(1) (a)



$F = \underbrace{B\bar{D} + \bar{A}C\bar{D} + A\bar{C}\bar{D}}_{\text{min SOP}} = B\bar{D} + (\bar{A}C + A\bar{C})\bar{D} = B\bar{D} + (A \oplus C)\bar{D}$

(b) (6,7) & (12,13)

(c) $F = B\bar{D} + \bar{A}C\bar{D} + AC\bar{D} + \bar{A}BC + AB\bar{C}$

(2) 8:1 → 8 data bits → $\lceil \log_2(8) \rceil = 3$ select bits

(7..0 ↑ data bits; 2..0 ↑ select bits ← 0-based)

$y = s_2\bar{s}_1\bar{s}_0 d_0 + s_2\bar{s}_1 s_0 d_1 + s_2 s_1 \bar{s}_0 d_2 + s_2 s_1 s_0 d_3$
$+ \bar{s}_2\bar{s}_1\bar{s}_0 d_4 + \bar{s}_2\bar{s}_1 s_0 d_5 + \bar{s}_2 s_1 \bar{s}_0 d_6 + \bar{s}_2 s_1 s_0 d_7$

3. (2 points) Recall that the carry-lookahead adder (CLA) uses propagate and generate signals $p_i = a_i + b_i$ and $g_i = a_i b_i$. For a 4-bit CLA, ***write*** the ***2-level*** carry out (c_4) equation in terms of the propagate and generate signals.
4. (2 points) Assume that gate delay τ = 50 ps. ***Approximate*** the speed (propagation delay) of ***both*** a 64-bit RCA ***and*** a CLA using 4, ***16-bit*** lookahead modules. By ***what factor*** is the CLA faster? Note: make reasonable approximations about the number of gate delays; your answer need not be exact.

(3) $C_4 = g_3 + g_2 p_3 + g_1 p_2 p_3 + g_0 p_1 p_2 p_3$ + c0p0p1p2p3

(4) RCA: 2 delays per bit → 128τ

CLA: bit p+g @ t = τ

block p+g @ t = 3τ

$C_{IN16, 32, 48}$ @ 5τ, 7τ, 9τ

RCA 48..63 starts @ ←, (9 + 16×2)τ = 41τ

factor of speedup: $\frac{128}{41} = 3.12\ldots$

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      3.12...
41 | 128
     123
     ---
       50
       41
       --
        90
        82
        --
         8
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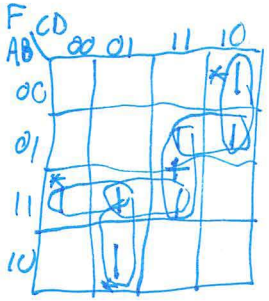
Name Answers

CE-1901-12 – Dr. Durant – Quiz 7
Fall 2016, Week 8 Quiz

1. (4 points) Glitches
   a. ***Derive*** the minimized SOP expression for F(ABCD) = $\Sigma_m(2,6,7,9,12,13,15)$.
   b. ***Determine*** between which pair(s) of minterms a (1-bit input change) glitch may occur.
   c. ***Modify*** the expression for F to avoid all glitches.
2. (2 points) ***Write*** the logic equation for the 8:1 MUX, y = f(s,d), where s and d are 0-based vectors of appropriate length. Remember that there is a product term for each of the data terms; this product term checks all values of s to make sure they match the term's corresponding s-minterm.

(1)(a)



$F = A\bar{B}\bar{C} + A\bar{C}D + \bar{A}C\bar{D} + BCD$

essential — simplest way to get 2 final minterms

(b) (6 & 7) & (13 & 15)

(c) $F = A\bar{B}\bar{C} + A\bar{C}D + \bar{A}C\bar{D} + BCD + ABD + \bar{A}BC$

ORIGINAL — glitch prevention

(2) 8:1 → data length = 8 → select length = $\lceil \log_2(8) \rceil = 3$

0..7 ↑ 0..2 ∈ 9-base!

$$y = \bar{s}_2\bar{s}_1\bar{s}_0 d_0 + \bar{s}_2\bar{s}_1 s_0 d_1 + \bar{s}_2 s_1 \bar{s}_0 d_2 + \bar{s}_2 s_1 s_0 d_3 + s_2\bar{s}_1\bar{s}_0 d_4 + s_2\bar{s}_1 s_0 d_5 + s_2 s_1 \bar{s}_0 d_6 + s_2 s_1 s_0 d_7$$

3. (2 points) Recall that the carry-lookahead adder (CLA) uses propagate and generate signals $p_i = a_i + b_i$ and $g_i = a_i b_i$. For a 4-bit CLA, ***write*** the ***2-level*** carry out (c_4) equation in terms of the propagate and generate signals.
4. (2 points) Assume that gate delay τ = 50 ps. ***Approximate*** the speed (propagation delay) of ***both*** a 64-bit RCA ***and*** a CLA using 16, ***4-bit*** lookahead modules. By ***what factor*** is the CLA faster? Note: make reasonable approximations about the number of gate delays; your answer need not be exact.

(3) ~~$c_4 = g_4 + g_3 p_4 + g_2 p_3 p_4 + g_1 p_2 p_3 p_4$~~

$c_4 = g_3 + g_2 p_3 + g_1 p_2 p_3 + g_0 p_1 p_2 p_3$ +c0p0p1p2p3

(4) RCA ~ 2 delays per bit, $64 \times 2\gamma = \boxed{128\gamma}$

CLA: bit p+g @ γ

block p+g @ 3γ — 2 layers

Fast carry ins: c_4 @ 5γ, c_8 @ 7γ

... c_{60} @ 33γ

Final RCA4 = $(33 + (4 \times 2))\gamma = \boxed{41\gamma}$

Factor = $\frac{128\gamma}{41\gamma} = \boxed{3.12\ldots}$

$$41 \overline{)128} \quad 3.12$$
$$123$$
$$50$$
$$41$$
$$90$$
$$82$$

i (c_i)	t
4	5γ
8	7γ
12	9γ
16	11γ
20	13γ
24	15γ
28	17γ
32	19γ
36	21γ
40	23γ
44	25γ
48	27γ
52	29γ
56	31γ
60	33γ

Fast carry @ $\left(\frac{i}{4} \cdot 2 + 3\right)\gamma$

layers per block

↑ /4 bits block