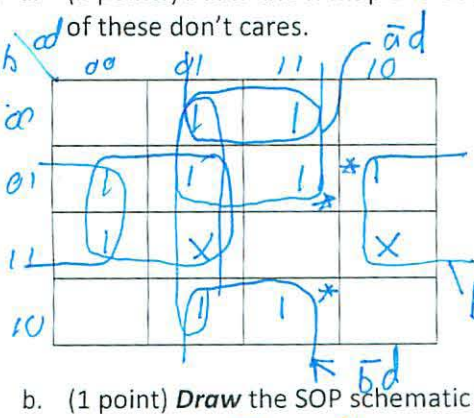
Name Answer

CE-1901 – Dr. Durant – Quiz 6
Fall 2015, Week 6 Quiz

1. (6 points) Simplification and implementation: $F(abcd) = \Sigma_m(1, 3, 4, 5, 6, 7, 9, 11, 12) + d(13, 14)$
   a. (2 points) ***Draw*** the K-map and use it to ***derive*** a simplified SOP expression taking advantage of these don't cares.



(-1/4 red. term)

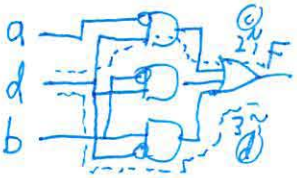
all 1's covered w/ essential PIs

$F = \bar{a}d + \bar{b}d + b\bar{d}$

c not needed!

There's omitted $\bar{a}\bar{b}$ for simplicity, but including it instead of $\bar{a}d$ is equally valid

   b. (1 point) ***Draw*** the SOP schematic using NOT-AND-OR gates.

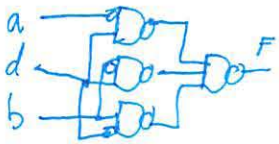


* even if all vars have NOT, any use w/o NOT since contamination delay of 2

   c. (0.5 point) ***What*** path of gates is involved in the contamination delay (shortest path) of this circuit? (illustrate in part b)
   d. (0.5 point) ***What*** path of gates is involved in the propagation delay (critical path) of this circuit? (illustrate in part b)
   e. (0.5 point) ***How*** many CMOS transistors does this require? Show your calculations.

2 NOT @ 2) 6) 32
3 AND2 @ 6) 18)
1 OR3 @ 8) 8)

   f. (1 point) ***Draw*** the NOT-NAND-NAND form of the SOP circuit. Hint: Begin by placing 2 NOTs in series on each input to the OR.



   g. (0.5 point) ***How*** many CMOS transistors does this require? Show your calculations.

3 NOT @ 2 = 6
3 NAND2 @ 4 = 12
1 NAND3 @ 6 = 6
24

   h. ***(0 points, extra challenge)*** Factor your result from (a) and apply bubble pushing to show how you can make an even smaller implementation of F than what you found above.

$F = d(\bar{a}+\bar{b}) + b\bar{d} = d\,\overline{\overline{a}\,\overline{b}} + b\bar{d} = \overline{\overline{d\,\overline{a}\,\overline{b}}} + \overline{\overline{b\bar{d}}} = \overline{d\,\overline{a}\,\overline{b}}\;\overline{b\bar{d}}$

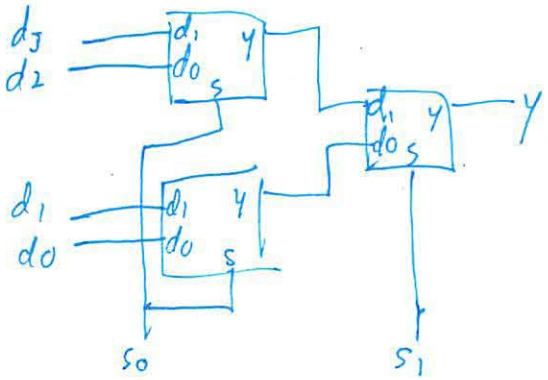
1 NOT @ 2 = 2
4 NAND2 @ 4 = 16
18

there is also $b \oplus d$, but XOR is a large gate in CMOS.

2. (2 points) MUXes
   a. (2 points) ***Write*** the logic equation for the 4:1 MUX, $y = f(s_{1..0}, d_{0..3})$. Remember that there is a product term for each of the data terms; this product term checks all values of s to make sure they match the term's corresponding s-minterm.

$$y = \bar{s}_1 \bar{s}_0 d_0 + \bar{s}_1 s_0 d_1 + s_1 \bar{s}_0 d_2 + s_1 s_0 d_3$$

   b. (2 points) Using a block diagram ***show*** how a 4:1 MUX can be made from 3, 2:1 MUXes.



(-1/4) s_1, s_0 reversed
(-1/2) internal signals mostly unlabeled

3. (2 points) Signed Numbers
   a. ***Calculate*** the range of a 12-bit ***signed*** number. Remember, half of the numbers are negative.

$2^{11} = 2048$ negative numbers, 1 zero, 2047 positives

[-2048, 2047]

don't negate, 2's comp. represents + & - numbers

   b. ***Convert*** +5 and -4 into their 4-bit 2's complement representations and confirm that their sum is +1.

5 0101 → flip 1010 → +1 1011

4 0100 → flip 1011 → +1 1100 → -4

```
  11
  0101   5
+ 1100  +-4
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 [0001]  1
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Name Answers

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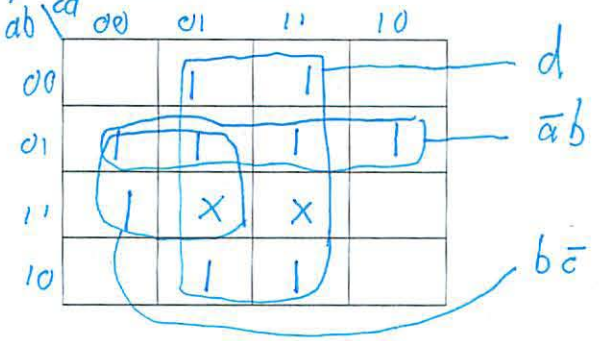
ALTERNATE PROBLEM → NOT GIVEN ON QUIZ

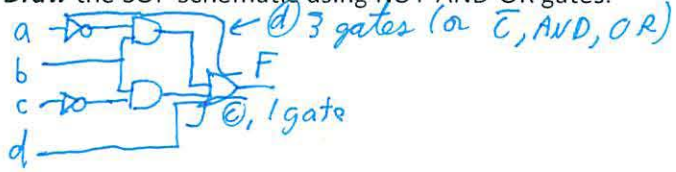
1. (6 points) Simplification and implementation: $F(abcd) = \Sigma_m(1, 3, 4, 5, 6, 7, 9, 11, 12) + d(\cancel{13}, \cancel{14}, 15) + d(14, 15)$

   a. (2 points) ***Draw*** the K-map and use it to ***derive*** a simplified SOP expression taking advantage of these don't cares.



$F = \bar{a}b + b\bar{c} + d$

   b. (1 point) ***Draw*** the SOP schematic using NOT-AND-OR gates.



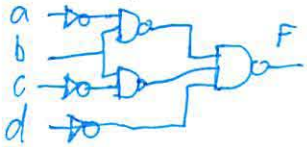
   c. (0.5 point) ***What*** path of gates is involved in the contamination delay (shortest path) of this circuit? (illustrate in part b)

   d. (0.5 point) ***What*** path of gates is involved in the propagation delay (critical path) of this circuit? (illustrate in part b)

   e. (0.5 point) ***How*** many CMOS transistors does this require? Show your calculations.

$2 \times 2 = 4$ for NOT
$2 \times 6 = 12$ for AND2
$1 \times 8 = 8$ for OR3
24

   f. (1 point) ***Draw*** the NOT-NAND-NAND form of the SOP circuit. Hint: Begin by placing 2 NOTs in series on each input to the OR.

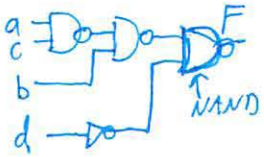


   g. (0.5 point) ***How*** many CMOS transistors does this require? Show your calculations.

$6 = 3 \times 2$ for NOT
$8 = 2 \times 4$ for NAND2
$6 = 1 \times 6$ for NAND3
20

   h. ***(0 points, extra challenge)*** Factor your result from (a) and apply bubble pushing to show how you can make an even smaller implementation of F than what you found in ~~(e)~~ above.

$F = b(\bar{a} + \bar{c}) + d = b\,\overline{ac} + d = \overline{\overline{b\,\overline{ac}}\;\overline{d}}$



$3 \times$ NAND2 → 12
$2 \times$ NOT → 2
14