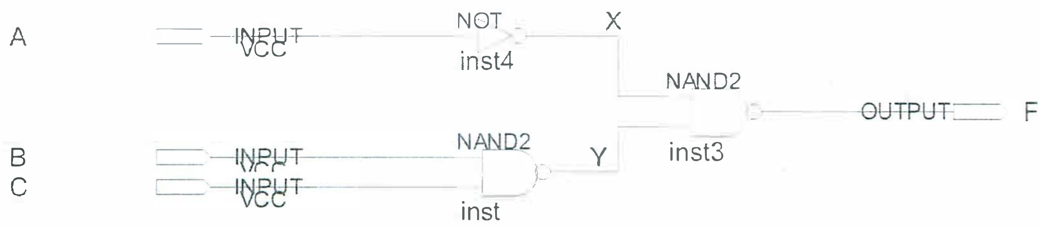
Name ~~Answers~~

CE-1901-11 – Dr. Durant – Quiz 4
Winter 2016-'17, Week 5

Note: These quiz problems are in 3 groups: problems 1-3, 4, and 5-8.

1. (2 points) **Complete** the truth table for the following schematic. **Include** columns for each intermediate term (all gate outputs).



A	B	C	X	Y	F
0	0	0	1	1	0
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	0	0	1

2. (1 point) **Write** the equation **directly** from the **schematic** above.

$\boxed{F = \overline{\overline{A}\ \overline{BC}}} = \overline{\overline{A}} + \overline{\overline{BC}} = A + BC$

3. (1 point) **Write** the simpler of the 2 canonical equations (SOP or POS) based on your truth table.

3 0s $\therefore$ POS is simpler

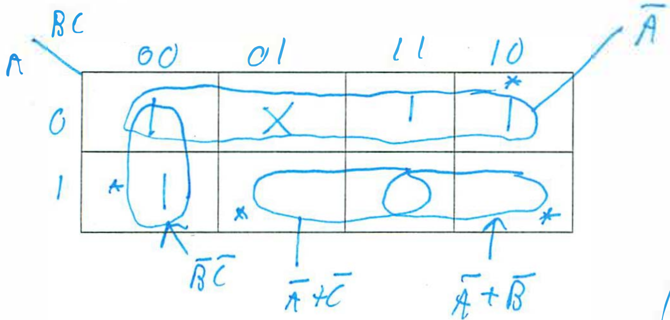
$F(ABC) = \prod(M_0, M_1, M_2) = M_0 M_1 M_2 = (A+B+C)(A+B+\overline{C})(A+\overline{B}+C)$

4. (1 point) **Prove** that (AB)' = A' + B' using perfect induction. That is, evaluate both expressions in a truth table and confirm that they agree in all rows. Be sure to include all intermediate terms as columns, including NOTs.

AB	$A \cdot B$	$\overline{A \cdot B}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
00	0	1	1	1	1
01	0	1	1	0	1
10	0	1	0	1	1
11	1	0	0	0	0

equal

5. (2 points) Let F(ABC) = $\Sigma_m(0,2,3,4) + d(1)$ (d indicates don't care conditions). Derive the simplest SOP or POS expression for F using a K-map. **Reminders**: adjacent terms in a K-map may differ in the value of only 1 bit. Start with m_0 in the upper left corner, putting m_1 to the right and m_4 below it. Form largest groups possible. It is okay to cover terms more than once as your form larger implicants.

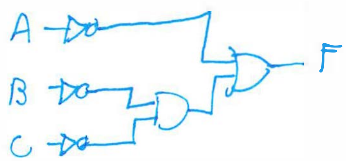


simplest (due to group of 4

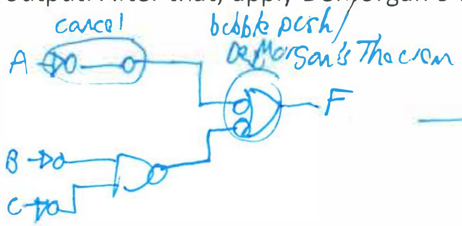
$\boxed{F = \bar{A} + \bar{B}\bar{C}} = (\bar{A}+\bar{C})(\bar{A}+\bar{B})$

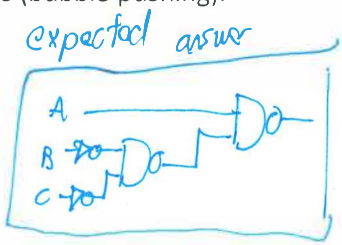
in Boolean algebra, + distributes over • (!)

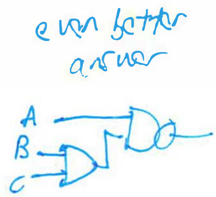
6. (1 point) Draw your reduced circuit for F directly using NOT, AND, and OR gates.



7. (1 point) Re-draw it using just (NAND [for SOP] or NOR [for POS]) and NOT gates based on the most simplified form. **Reminders:** The first step is to put 2 NOT gates on every input to the final output. After that, apply DeMorgan's Theorems (bubble pushing).







8. (1 point) ***Calculate*** the number of transistors needed for ***each*** of the two reduced circuits ~~equations~~ above.

(6)
3 NOT 6
1 AND2 6
1 OR2 6
18

(7) Expected
2 NOT 4
2 NAND2 8
12

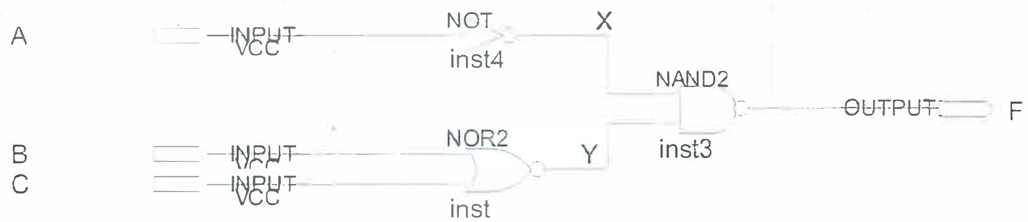
Better
1 OR2 6
1 NAND2 4
10

Name *Answers*

CE-1901-12 – Dr. Durant – Quiz 4
Winter 2016-'17, Week 5

Note: These quiz problems are in 3 groups: problems 1-3, 4, and 5-8.

1. (2 points) **Complete** the truth table for the following schematic. **Include** columns for each intermediate term (all gate outputs).



A	B	C	X	Y	F
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	0	1	1
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	0	1

2. (1 point) **Write** the equation **directly** from the **schematic** above.

$$\boxed{F = \overline{\bar{A}\,\overline{B+C}}} = \bar{\bar{A}} + \overline{\overline{B+C}} = A+(B+C) = A+B+C$$

3. (1 point) **Write** the simpler of the 2 canonical equations (SOP or POS) based on your truth table.

only 1 0, use POS

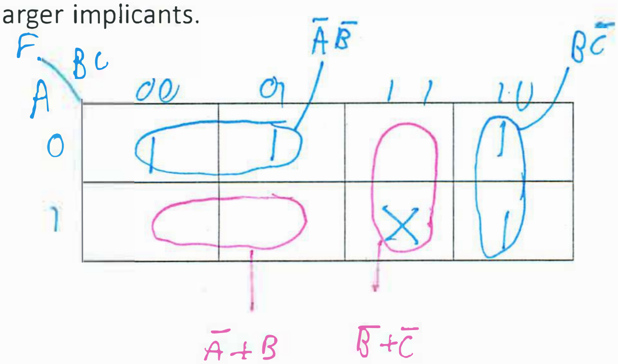
$F = A+B+C$ (1 ~~product~~ sum term, canonical)

4. (1 point) **Prove** that (A+B)' = A'B' using perfect induction. That is, evaluate both expressions in a truth table and confirm that they agree in all rows. Be sure to include all intermediate terms as columns, including NOTs.

A	B	$A+B$	$\overline{A+B}$	$\bar{A}$	$\bar{B}$	$\bar{A}\bar{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

Equal

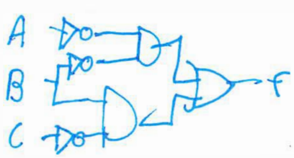
5. (2 points) Let F(ABC) = $\Sigma_m(0, 1, 2, 6) + d(7)$ (d indicates don't care conditions). Derive the simplest SOP or POS expression for F using a K-map. **Reminders**: adjacent terms in a K-map may differ in the value of only 1 bit. Start with m_0 in the upper left corner, putting m_1 to the right and m_4 below it. Form largest groups possible. It is okay to cover terms more than once as your form larger implicants.



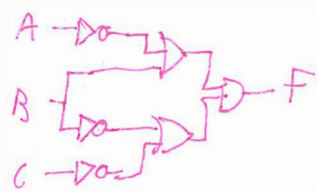
$F = \bar{A}\bar{B} + B\bar{C}$
$= (\bar{A}+B)(\bar{B}+\bar{C})$

equally complex either is correct

6. (1 point) Draw your reduced circuit for F directly using NOT, AND, and OR gates.

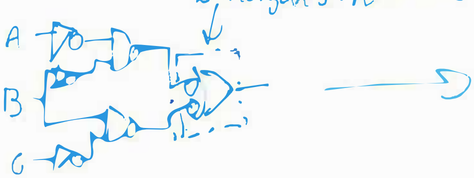


or



7. (1 point) Re-draw it using just (NAND [for SOP] or NOR [for POS]) and NOT gates based on the most simplified form. **Reminders:** The first step is to put 2 NOT gates on every input to the final output. After that, apply DeMorgan's Theorems (bubble pushing).

following SOP...
bubble push/
DeMorgan's Theorem



8. (1 point) ***Calculate*** the number of transistors needed for ***each*** of the two reduced circuits above.

6 SOP			7		
3 NOT	6		3 NOT	6	
2 AND2	12		3 NAND2	12	
1 OR2	6				
	24			18	