Name Unswers

CE-1901-11 - Dr. Durant - Quiz 3 Fall 2016, Week 3

- (1 point) Explain why a digital circuit might not operate properly if V_{OH} < V_{IH}.
- (1 point) Explain why a digital circuit might not operate properly if V_{0H} < V_{1H}.
 The voltage of an output of / is guaranteed to be at best VoH.
 Zet it evactly equal Vot. When received, the signal is interpoted as / if it is at least Vot. When received, the signal is Vot = V ± H.
 Bat, we are given VoH < V ± H, which is contradictory. Therefore, we did not receive a value of / is contradictory.
 (2 points) State and explain why either a (relatively) positive or negative charge must present at
- the gate of an NMOS transistor (specifically, an n-channel enhancement mode MOSFET [metaloxide-semiconductor field-effect transistor]) in order for current to *flow* between the drain and

positive charge, attracts negative electrons into the channel, allowing electrical current to flow since this is an M - channel FET the source?

3. (2 points) Complete a truth table for function that outputs 1 iff the 3-bit input, a₂a₁a₀ is a palindrome (it reads the same left-to-right as it does right-to-left).

a ₂	a ₁	a ₀	r
0	0	0	1
0	0	1	0
0	7	0	1
\mathcal{O}	1	1	0
1	0	0	0
1	\mathcal{O}^{\cdot}	1	1
1	1	0	0
1	1]	1

4. (1 point) Write the canonical sum-of-products (SOP) equation for your truth table.

N= a2a, a0+ a2a, a0 + a2a, a0+ a2a, a0

(= a20 a, but this is not canonica)

5. (1 point) Write the canonical SOP equation in sum-of-minterms (Σ) form.

 $\sim (a_2 a_1 q_d) = \mathcal{Z}_{m}(0, 1, 5, 7)$

6. (1 point) Draw the gate diagram for your canonical SOP equation.



7. (2 points) Draw an **ideal timing diagram** (like Quartus simulation output) for your function with the input progressing through all possible values in a logical order.



Name *Unsweis*

CE-1901-12 - Dr. Durant - Quiz 3 Fall 2016, Week 3

1. (1 point) Explain why $V_{OL} < V_{IL}$ is a requirement for the proper operation of a digital circuit.

If the condition is violated then the transmitted voltage representing a & can be higher them the movemin acceptable value for a receiver to interpret it as a &, realities in representing in the interpret it as a & realities in an incorrect interpretation

2. (2 points) Explain what it means to say that transistors are active devices (as opposed to passive devices). Recalling the light switch example might be helpful.

They control a "owitch energy that can be greater than the input energy used for control. (Thus they require a separate source from the controlling

3. (2 points) **Complete** a truth table for function that outputs 1 iff the 3-bit unsigned number, a2a1a0, is less than 4.

a ₂	a ₁	a ₀	r
0	0	0	1
0	0	7	1
0	t	0	1
0	1	1	1
1	0	0	Ø
1	0	1	0
1	1	0	0
/	1)	C

4. (1 point) Write the canonical sum-of-products (SOP) equation for your truth table.

N= q2q, a0 + a 2q, q0+ a2q, a0+ a2q, a0

(=az, but that not conomic

5. (1 point) Write the canonical SOP equation in sum-of-minterms (Σ) form.

~(a2,a1,a0)= Em(0,1,2,3)

6. (1 point) Draw the gate diagram for your canonical SOP equation.



7. (2 points) Draw an **ideal timing diagram** (like Quartus simulation output) for your function with the input progressing through all possible values in a logical order.

